Silicon Detectors

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Historical aspects – Why use silicon?

- Since 50ies large crystals for energy measurements
- Need for fast and precise position measurements

Where are silicon sensors better suited than gas detectors?
Fast ~O(10ns); Precise O(5µm); very good energy resolution ~O(eV)

  - 80ies charm quark tagging
  - Late 80ies LEP experiments, vertex tracker
  - 90ies in hadron machines FERMILAB
  - Today in all LHC experiments

Silicon detectors gives vertexing, which gives
- b tagging
- lifetimes
- mixing background suppression

…… and a lot of great physics!

Why wasn't silicon used earlier?
- Needed micro-lithography technology ⇒ cost
- Small signal size (need low noise amplifiers)
- Needed read-out electronics miniaturization
  - (transistors, ICs)

Historical aspects II – Why use silicon?

the post era of the *Z and W discovery, after the observation of Jets at UA1 and* UA2 at CERN, John Ellis visioned at a HEP conference at Lake Tahoe, California in 1983 “To proceed with high energy particle physics, one has to tag the flavour of the quarks!”

CDF; top quark discovery

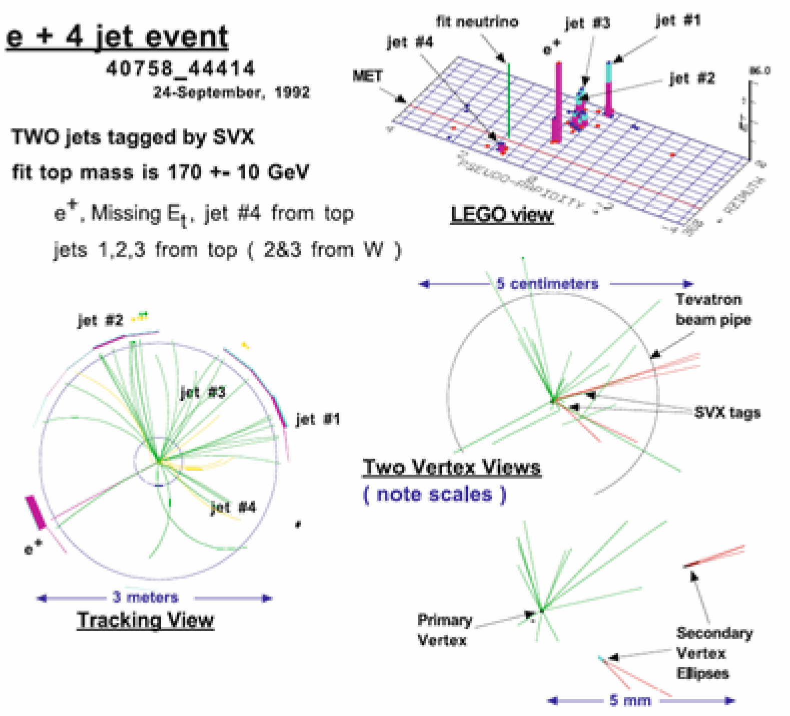
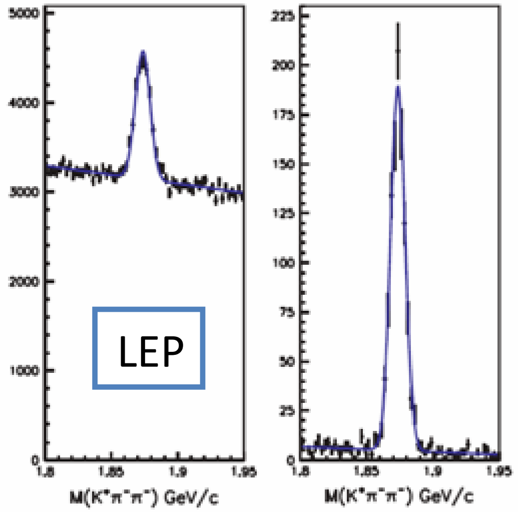
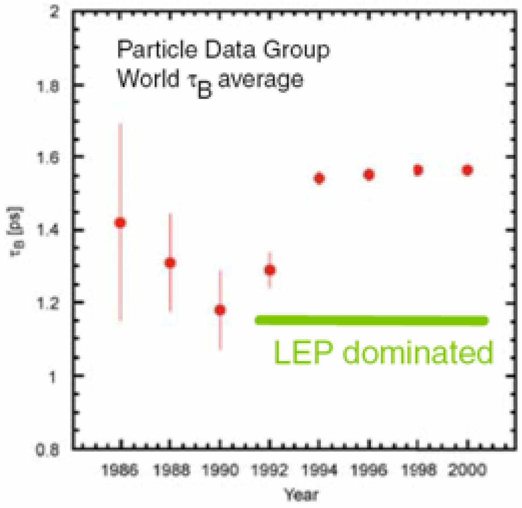


Fig. 4.23 A “Golden” t event. $t\bar{t}$ decaying into W^+b, $W^-\bar{b}$, where one W decays leptonically with the signature lepton ID plus missing energy, the second W decays into $q\bar{q}$ resulting in two jets together with the initial two tagged b jets. In total one lepton, four jets, two tagged b jets and missing energy were reconstructed [151]

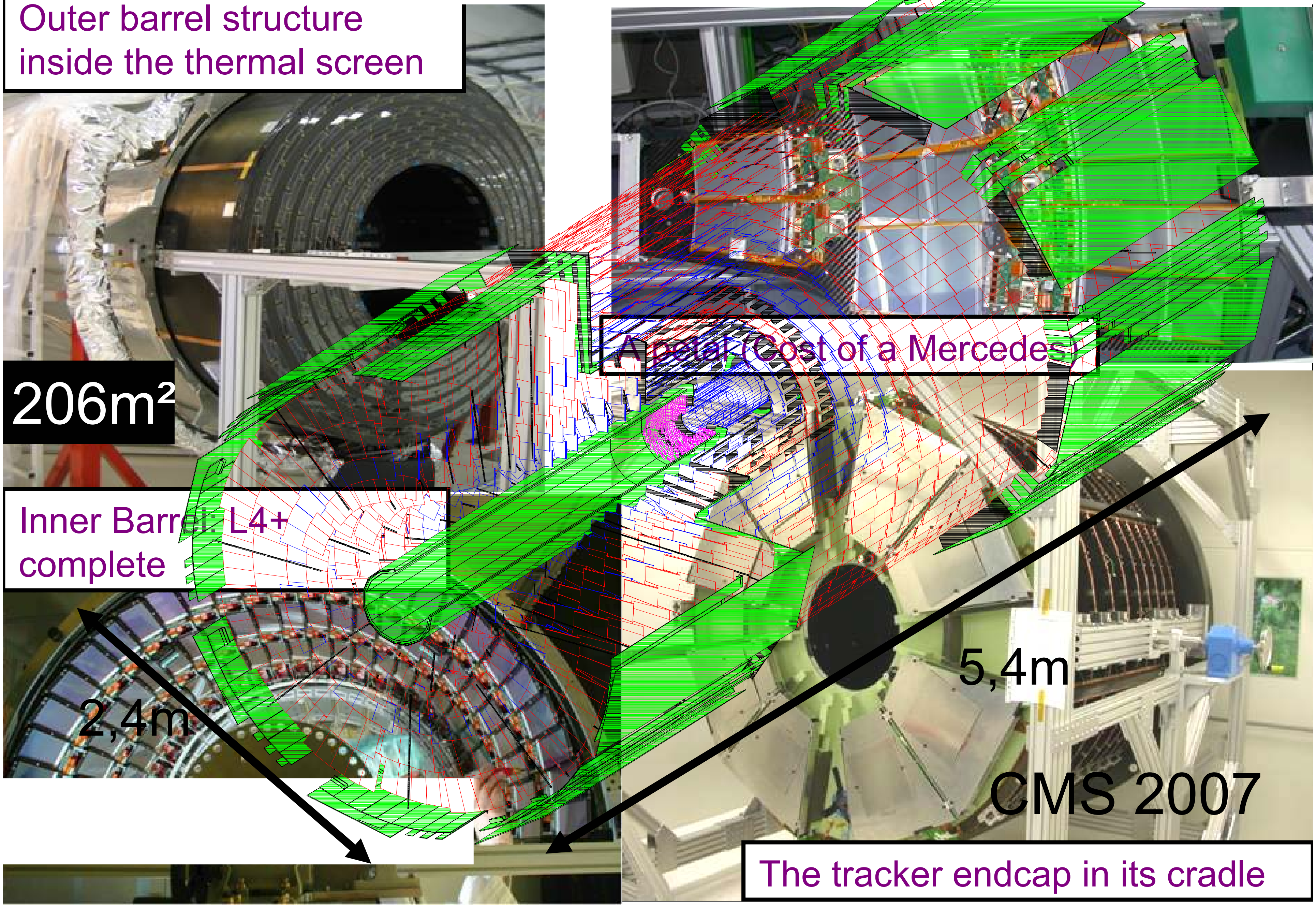


LEP



Background reduction

CMS –some pictures from construction



Outer barrel structure inside the thermal screen

Inner Barrel: L4+ complete

A petal (Cost of a Mercedes)

The tracker endcap in its cradle

Why Use Silicon II

- We benefit from the huge technological advances in the IT industry
  - Pattern and structuring is industry standard
- Even if the infrastructure is expensive, the basic ingredients are ridiculously cheap and exist in abundance

The usefulness and success of silicon technology can be explained in a handful of keywords:

- *existence in abundance*
- *energy band gap*
- *possibility to change gap properties by defined adding of certain impurity atoms* (dopants)
- ***the existence of a natural oxide***

Silicon properties

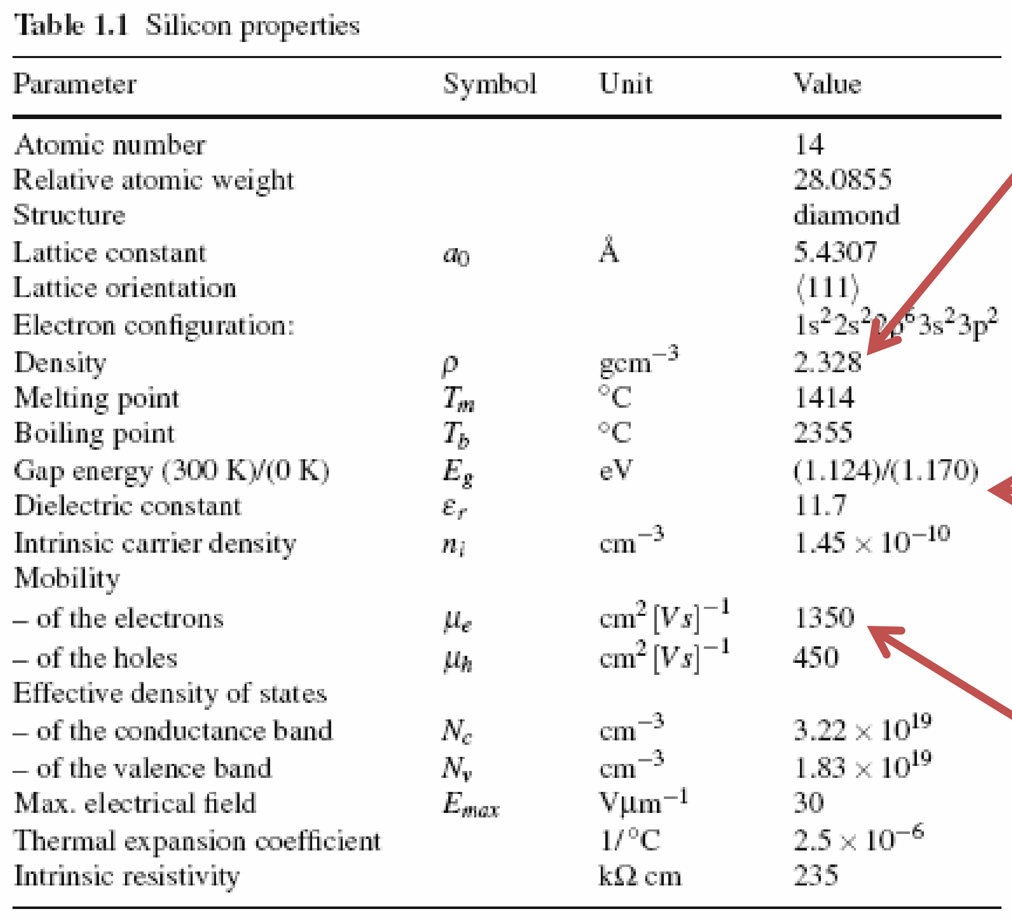


Table 1.1 Silicon properties

Parameter	Symbol	Unit	Value
Atomic number			14
Relative atomic weight			28.0855
Structure			diamond
Lattice constant	a_0	Å	5.4307
Lattice orientation			$\langle 111 \rangle$
Electron configuration:			$1s^2 2s^2 2p^6 3s^2 3p^2$
Density	ρ	gcm^{-3}	2.328
Melting point	T_m	°C	1414
Boiling point	T_b	°C	2355
Gap energy (300 K)/(0 K)	E_g	eV	(1.124)/(1.170)
Dielectric constant	ε_r		11.7
Intrinsic carrier density	n_i	cm^{-3}	1.45×10^{-10}
Mobility			
– of the electrons	μ_e	$\mathrm{cm}^2\,[Vs]^{-1}$	1350
– of the holes	μ_h	$\mathrm{cm}^2\,[Vs]^{-1}$	450
Effective density of states			
– of the conductance band	N_c	cm^{-3}	3.22×10^{19}
– of the valence band	N_v	cm^{-3}	1.83×10^{19}
Max. electrical field	E_{max}	$\mathrm{V\mu m}^{-1}$	30
Thermal expansion coefficient		1/°C	2.5×10^{-6}
Intrinsic resistivity		kΩ cm	235

And detector relevant:

- Dense: the average energy loss and high ionized particle number with 390eV/*µm* ~ *108 (electron–hole pairs)/µm is effectively high due to the high* density of silicon.
  - No charge amplification needed
- very good intrinsic energy resolution: for every 3.6 eV released by a particle crossing the medium, one electron–hole pair is produced. (30 eV to ionize a gas molecule)
- Very fast O(10ns)
- Mechanical stability
  - Self supporting

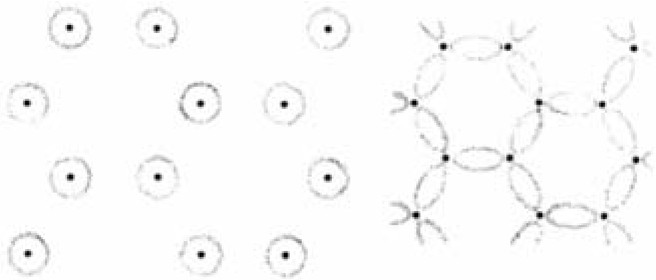
ρ(Si)=2.33g/cm³ with Bethe-Bloch dE/dx=1.664MeV/gcm^{-2} (MIP) one gets per 300µm:

N=300µm*1.664MeV/gcm^{-2}*2.33g/cm³/3.6ev= 32000 e-h pairs per 300µm

HOW DO SILICON SENSORS WORK?

Basic Solid State Physics: Energy Bands
Semiconductor: Band Gap

When isolated atoms are brought together to form a lattice, the discrete atomic states shift to form energy bands



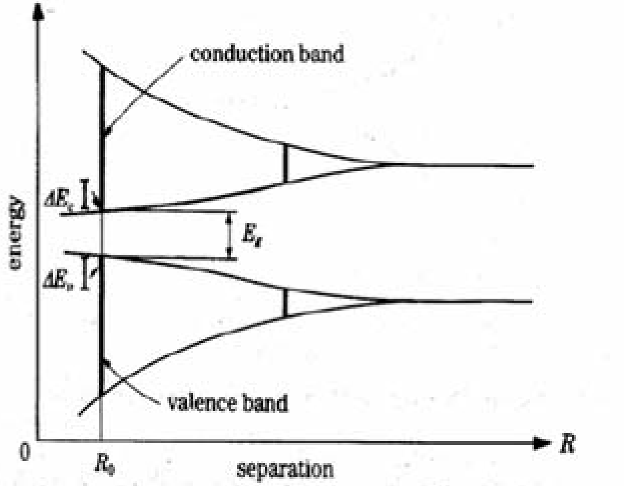
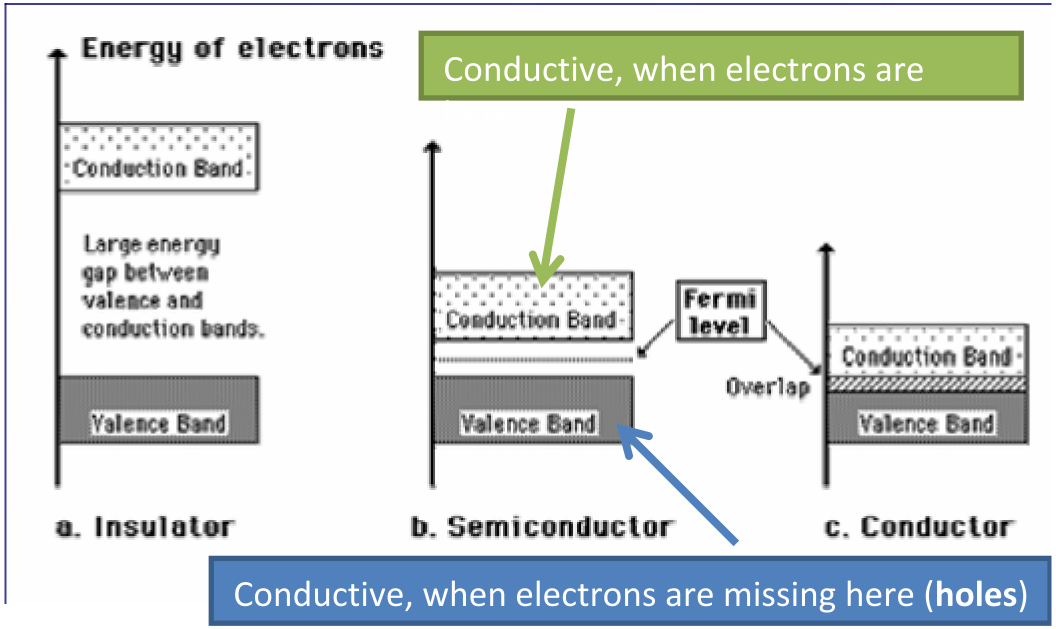


Fig. 1.3. Energy levels in a system of N atoms as a function of the separation R between the atoms. The equilibrium atomic separation is R_0.



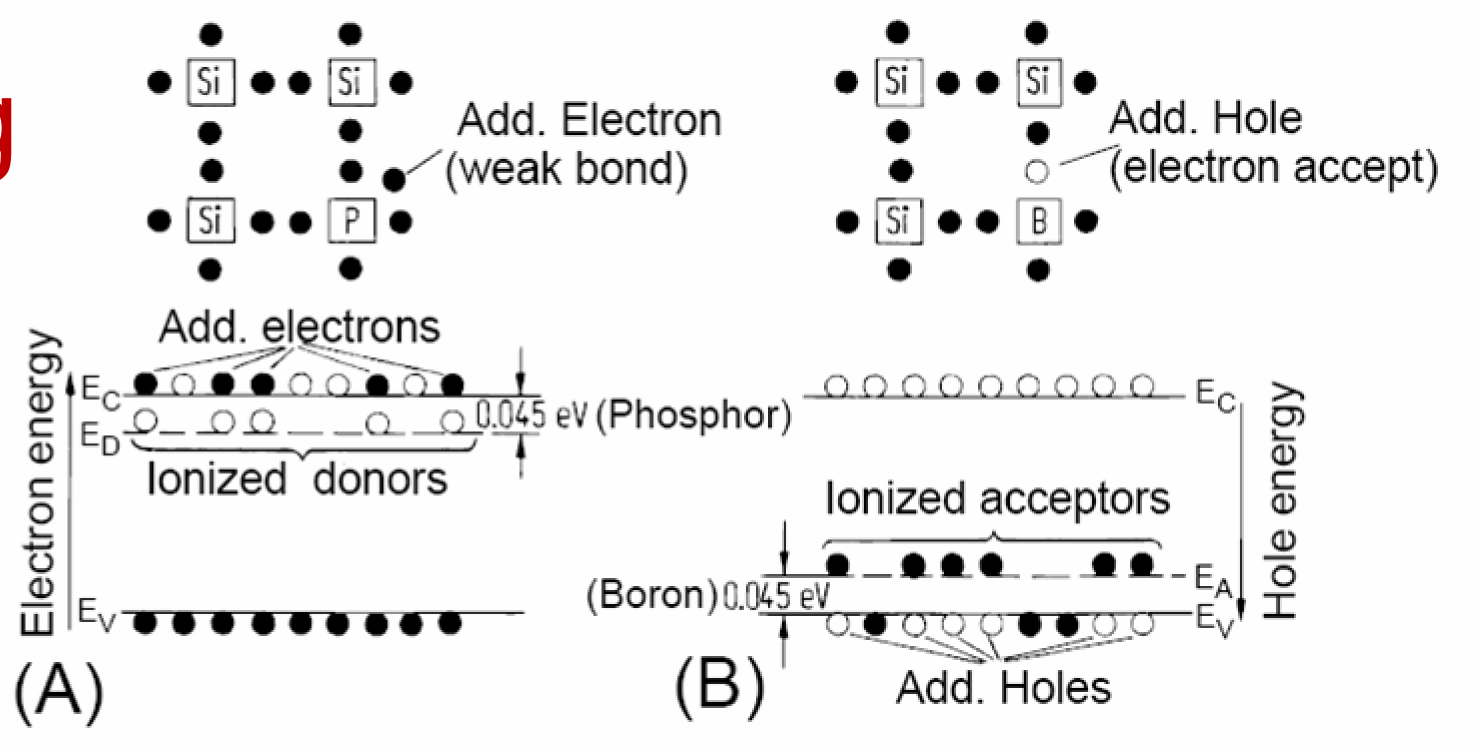
Conductive, when electrons are

Conductive, when electrons are missing here (**holes**)

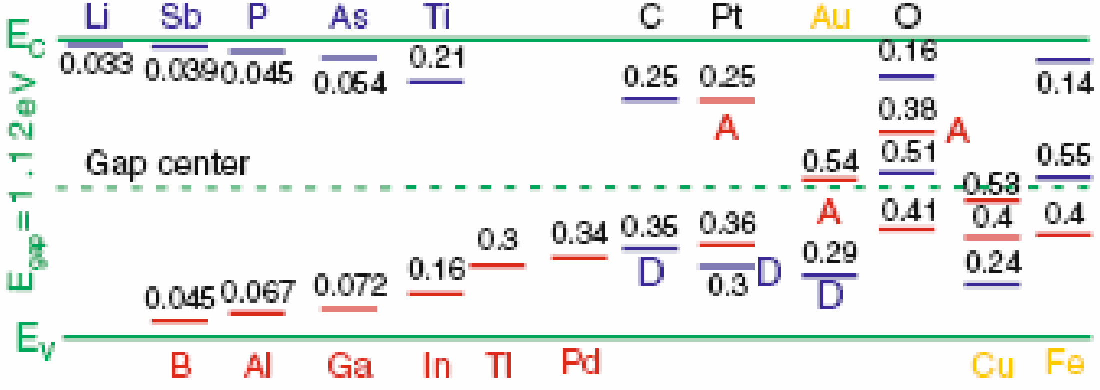
When the gap is large, the solid is an insulator.
If there is no gap, it is a conductor.
A semiconductor results when the gap is small.

Ge	0.7 eV
GaAs	1.4 eV
Si	1.1 eV
Diamond	4.5 eV (insulator)

Doping



New energy levels



Typical concentration levels are

- Si atoms $5 \times 10^{22}\,\mathrm{cm}^{-3}$
- $n_i = 1.45 \times 10^{10}\,\mathrm{cm}^{-3}$ at 27°C
- HEP silicon sensor n-bulk $10^{12}\,\mathrm{cm}^{-3}$
- HEP strip/pixel implant doping 10^{14}–$10^{16}\,\mathrm{cm}^{-3}$
- light doping (IC industry) $10^{16}\,\mathrm{cm}^{-3}$
- heavy doping (IC industry) $10^{19}\,\mathrm{cm}^{-3}$

➔ Dedicated material tuning possible!

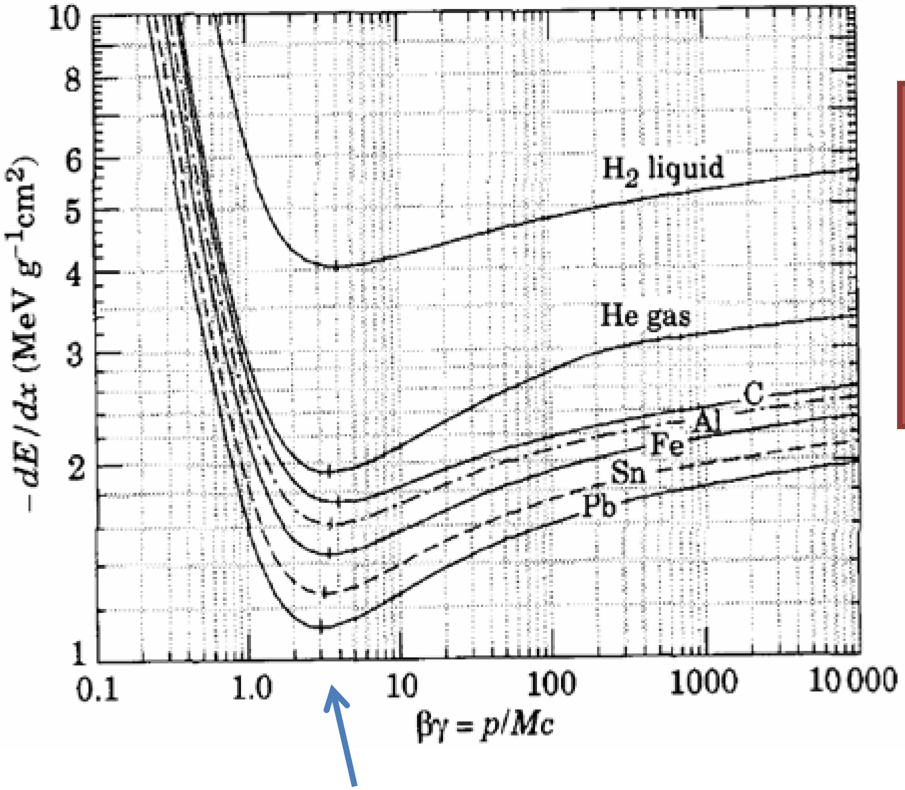
Ionization: Bethe-Bloch-Formula

Coulomb interaction

Energy deposit of traversing charged particle per unit length

➔ Ionisation (Ions, electron-hole pairs are recorded)

$$-\left(\frac{dE}{dx}\right)_{coll} = 2\pi N_A r_e^2 m_e c^2 \rho \frac{Z}{A}\frac{z^2}{\beta^2} \cdot \left[\ln\left(\frac{2m_e c^2 \gamma^2 \beta^2 W_{max}}{I^2}\right) - 2\beta^2 - \delta - 2\frac{C}{Z}\right]$$



Minimal ionising particle MIP

Now in Si, this elevates an e from the valence band to the conduction band

➔Electron-hole pair (e-h)

➔MIP in 300µm thick silicon around 30.000 e-h

1. Now, we place a piece of silicon

OK?

2. Then we wait for a passing charged ionizing particle ➔ creating an electron hole pair (Bethe-Bloch)
3. Then we collect the e-h pair! ☺

4. But wait! How do we collect the e-h pair?
5. How do we distinguish the 10^4 created e-h within the existing 10^{12} free charge carriers (at room temperature)?
6. Don‘t these e-h pair recombine?

Free charge carriers $$n_i = \sqrt{N_C N_V} \cdot \exp\left(-\frac{E_g}{2kT}\right) \propto T^{\frac{3}{2}} \cdot \exp\left(-\frac{E_g}{2kT}\right)$$

7. We could cool the solid, but that is technically complicated

➔ We have to deplete the volume from free charge carriers!

& We have to collect the created charge

➔ we establish a pn-junction

pn-junction (diode)

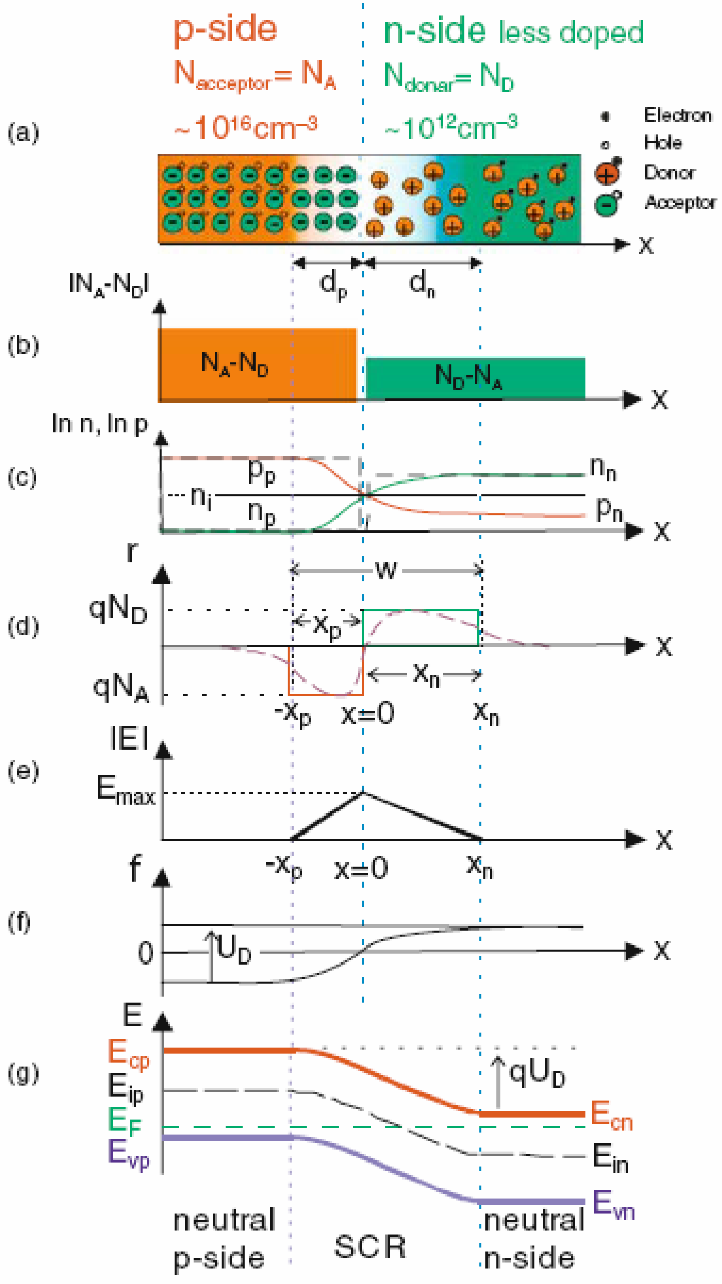


Fig. 1.5 These diagrams display (**a**) a simple visualization of the atomic and charge configuration, (**b**) the doping profile, (**c**) the mobile charge density, (**d**) the space charge density, (**e**) the electrical field configuration, (**f**) the electrical potential, (**g**) electron energy across the pn-junction. All states are depicting the equilibrium state, without any external voltage

Poisson equation describes the electrostatic potential $\phi(x)$:

$$\frac{\partial^2\phi}{\partial x^2} = -\frac{1}{\varepsilon_{SC}\varepsilon_0}\varrho(x)$$

$$\varrho(x) = -q[n(x)-p(x)+N_A-N_D]$$

$$\boxed{|E_n(x)|} = +\frac{qN_D}{\varepsilon_{SCR}\varepsilon_0}\boxed{(x+x_n)}; \qquad |E_p(x)| = +\frac{qN_A}{\varepsilon_{SCR}\varepsilon_0}(x-x_p)$$

$$\boxed{\phi_n(x)} = -\frac{1}{2}|E_{max}|x_n\cdot\left[\boxed{\left(\frac{x}{x_n}\right)^2}+2\frac{x}{x_n}\right]; \qquad \phi_p(x) = +\frac{1}{2}|E_{max}|x_p\cdot\left[\left(\frac{x}{x_p}\right)^2-2\frac{x}{x_p}\right]$$

The total difference of potential in the space charge region gives the **diffusion or built-in voltage** $V_{diffusion}$

$$V_{diffusion} = \phi_p(+x_p)-\phi_n(-x_n) = \frac{1}{2}\,|\,E_{max}\,|\,w \overset{eq.\ 1.9,\ 1.14}{=} \frac{1}{2\mu\varrho\varepsilon}w^2 \qquad (1.16)$$

$V_{diffusion}$ is ~O(mV), w ~O(μm)

Not sufficient!

Reverse and Forward Bias Voltage

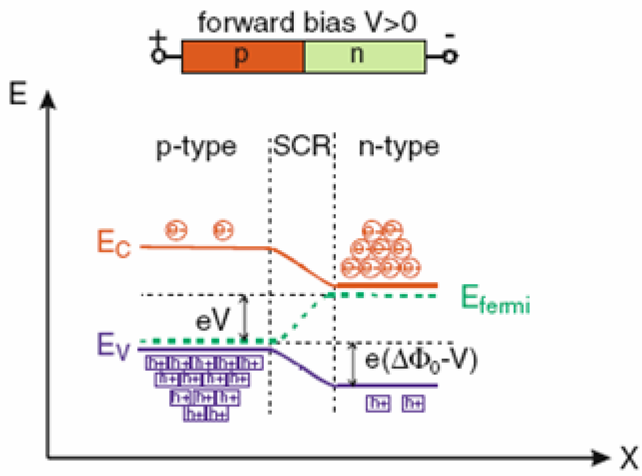


Fig. 1.6 Forward (bias) voltage: In the forward case, the barrier decreases significantly, the majority carriers flow freely through the diode

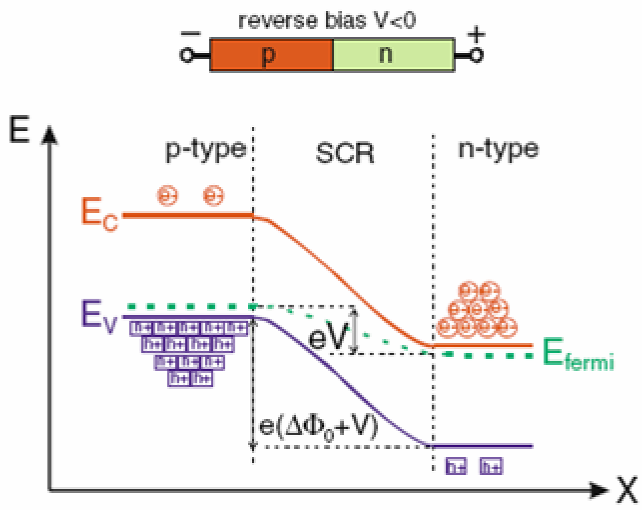


Fig. 1.7 Reverse (bias) voltage: In the reverse bias case, the potential barrier as well as the depletion width increases

To enlarge the SCR region, an external voltage is applied on top of $V_{diffusion}$

➔

$$\boxed{w = \sqrt{2\varepsilon \varrho \mu V_{bias}}}$$

- The voltage needed to completely deplete a device of thickness d is called the depletion voltage $V_{full\ depletion} = V_{FD}$

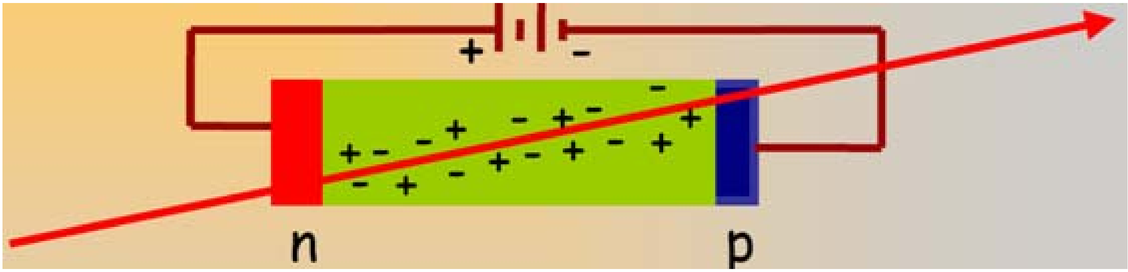
$$\boxed{V_{full\ depletion} = V_{FD} = \frac{D^2}{2\varepsilon \mu \varrho}}$$

➔

- Reverse bias diode = no free charge carriers
- Electrical field helps to „drain/collect“ the created charges (e-h)

From Diode to Strip or Pixel Sensor

- Now we have a diode

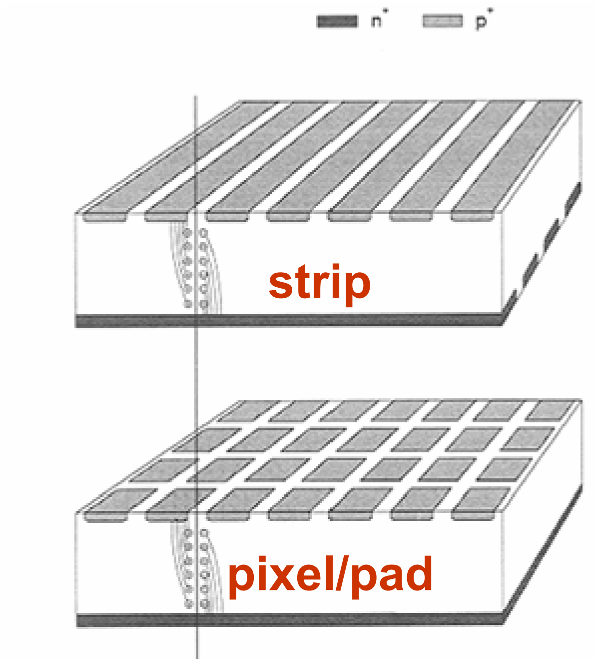


➔ Produce more diodes!

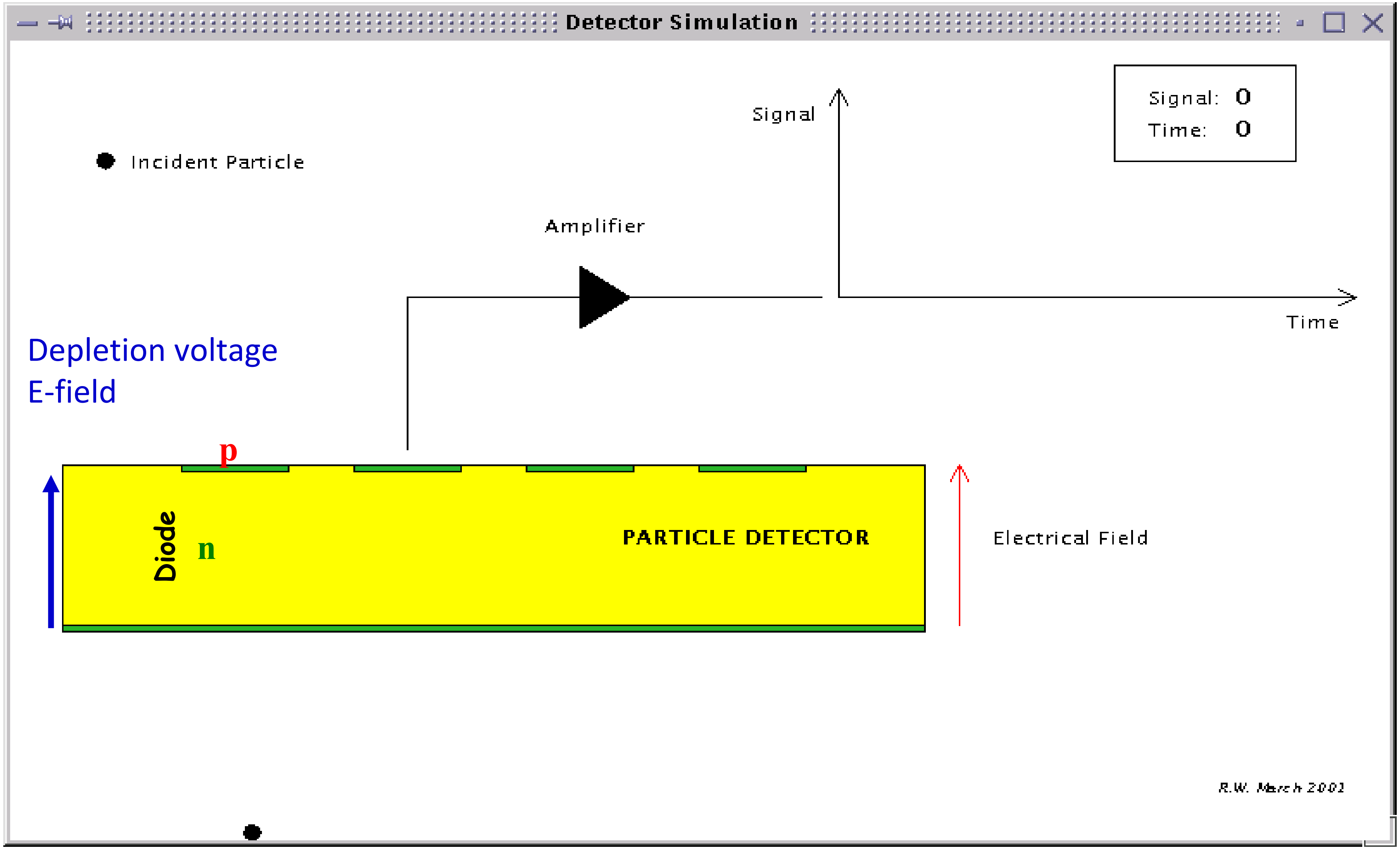
➔ Better: produce more diodes on a single substrate

= Create a pattern on the substrate

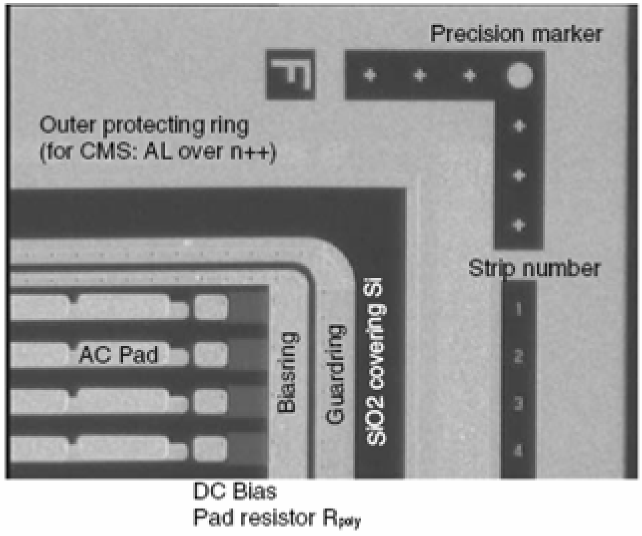
Reverse bias the pattern individually



Functioning principle



Real life strip detector



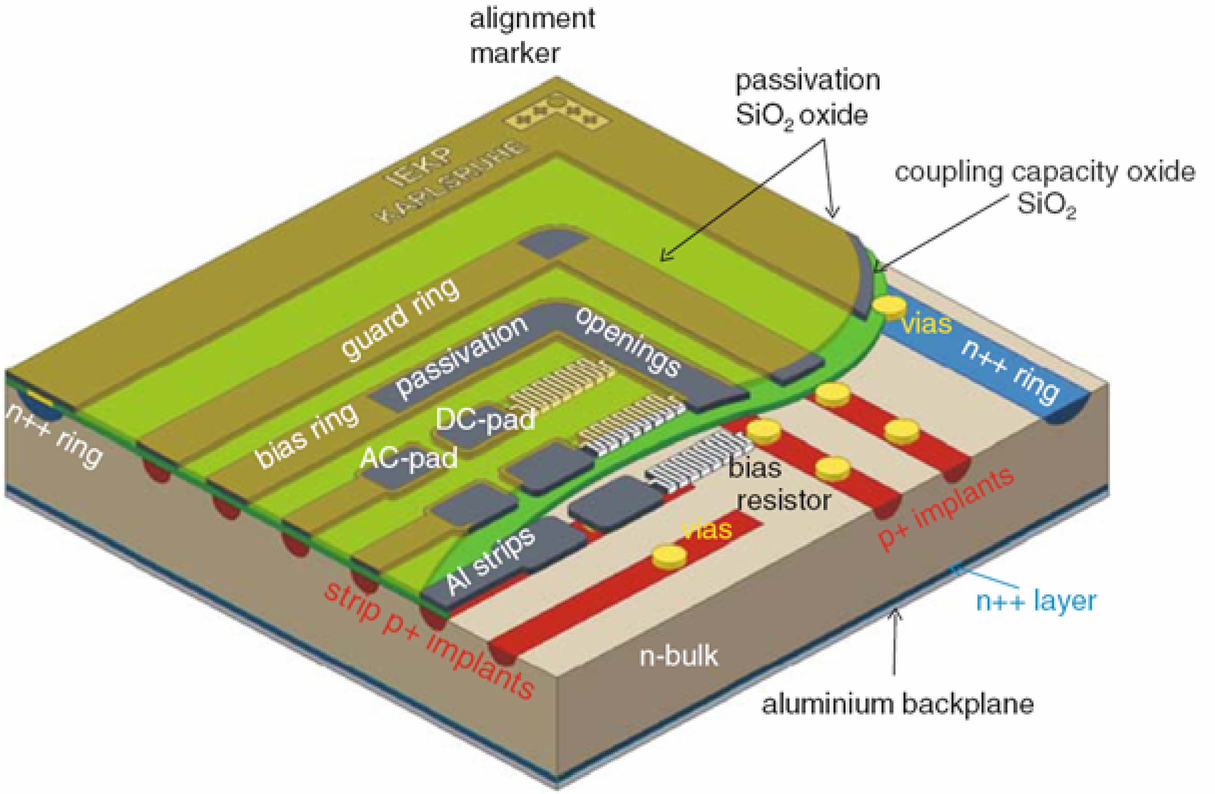


Fig. 1.19 A 3D schematic is sketched. It shows the baseline of the CMS sensor at the LHC in 2008, but could represent basically any single-sided AC-coupled, R_{poly} biased sensor. In operation, the bias ring is connected to GND potential, which is then distributed to the p+ implant strips, while the Al backplane is set to positive high voltage depleting the full n-bulk volume by forming a pn-junction p+ strip to n-bulk. The coupling capacitor is defined between aluminium strip and p+ implant, the inter-strip capacity between neighbouring strips (both p+ and Al part). The guard ring shapes the field at the borders. The n++ ring defines the volume and prevents high field in the real cut edge regions

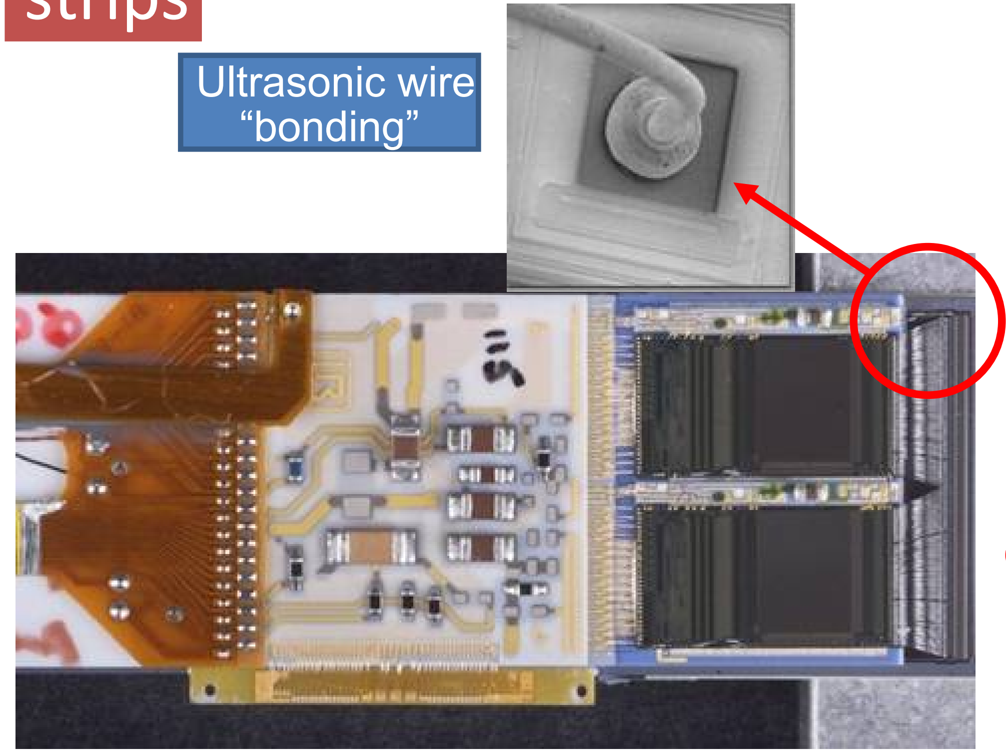
Disclaimer:
This lecture does not detail the individual strip parameters nor signal, noise or electronics

Silicon Pixel

- Principle similar to silicon strip sensors
- Segmentation: Pixel(-diodes) instead of Strip(-diodes)
  - Electronic on top of sensor to reach all pixels

strips

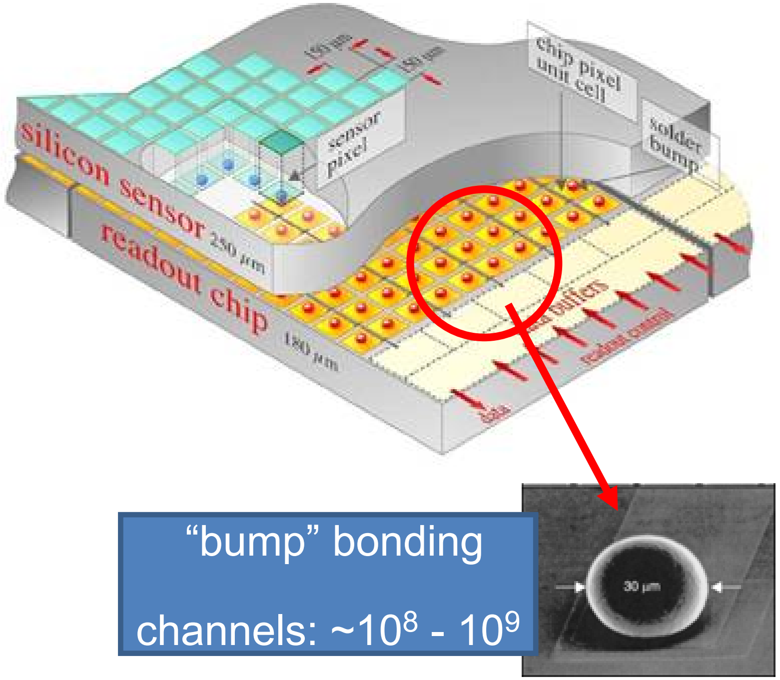
Ultrasonic wire
“bonding”



Sensor

strips: just ONE coordinate,
Pixel: two coordinates 2D

pixel



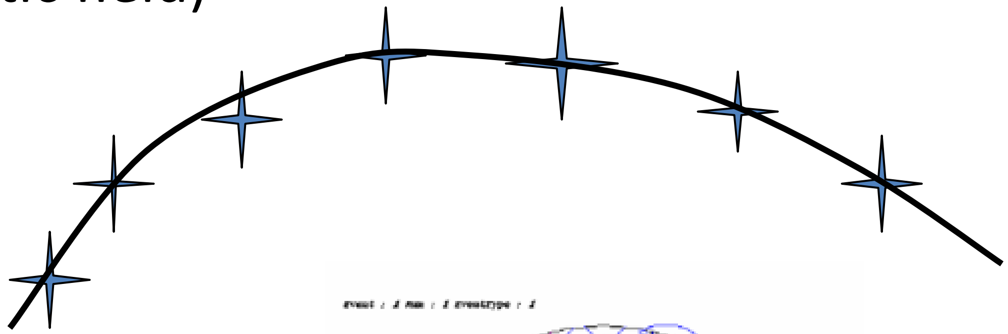
“bump” bonding

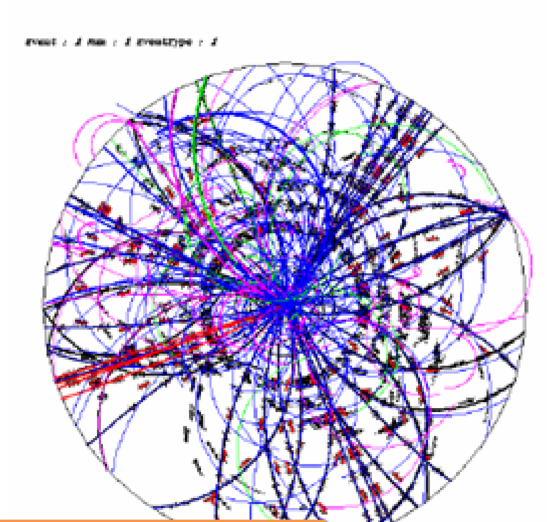
channels: ~10^8 - 10^9

FULL SILICON DETECTORS

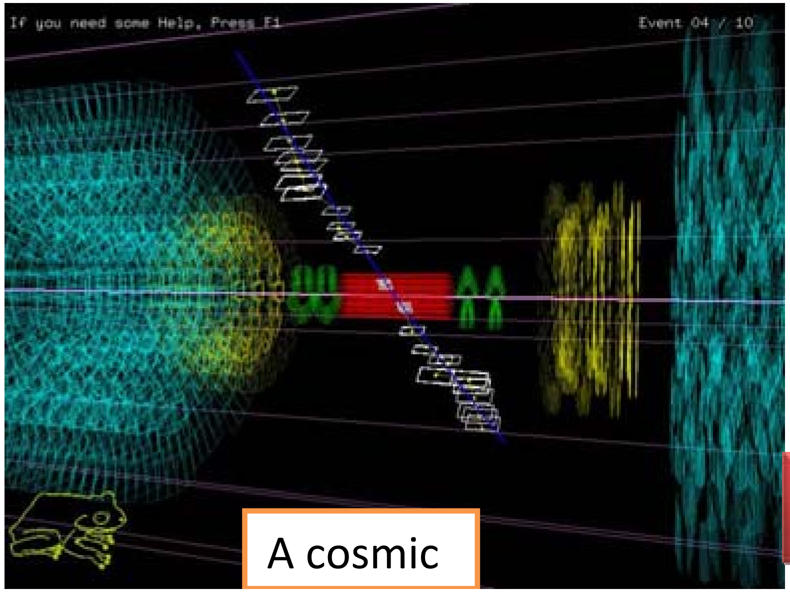
Many of These Structured Devices Form a Tracking Detector

- We measure
  - Momentum (with magnetic field)
  - Tracks
  - Decay points
    - Life time
    - Flavour tagging





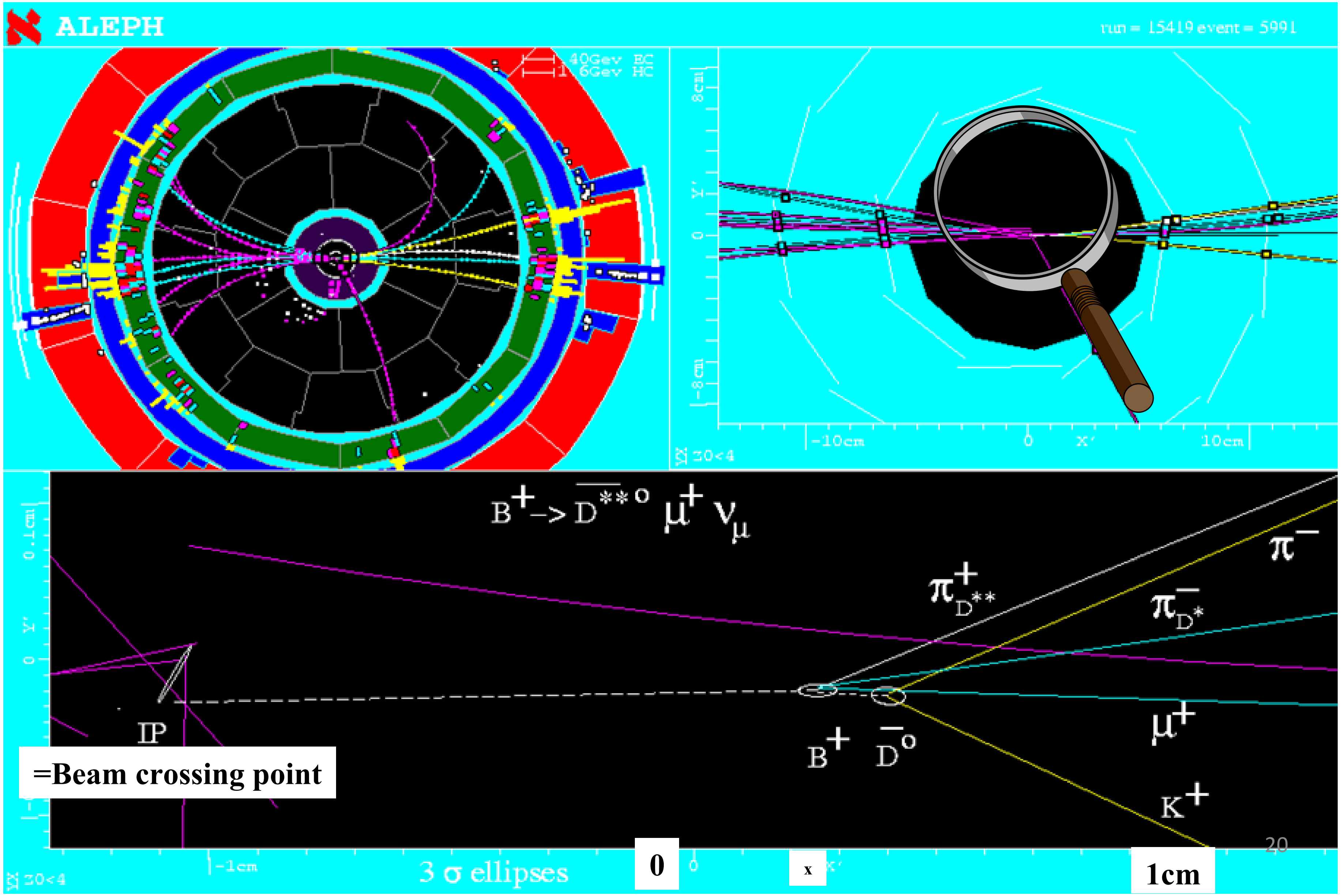
A simulated event



A cosmic

Resolution in the order of some µm

Do we need such a high resolution?



A “simplified” description

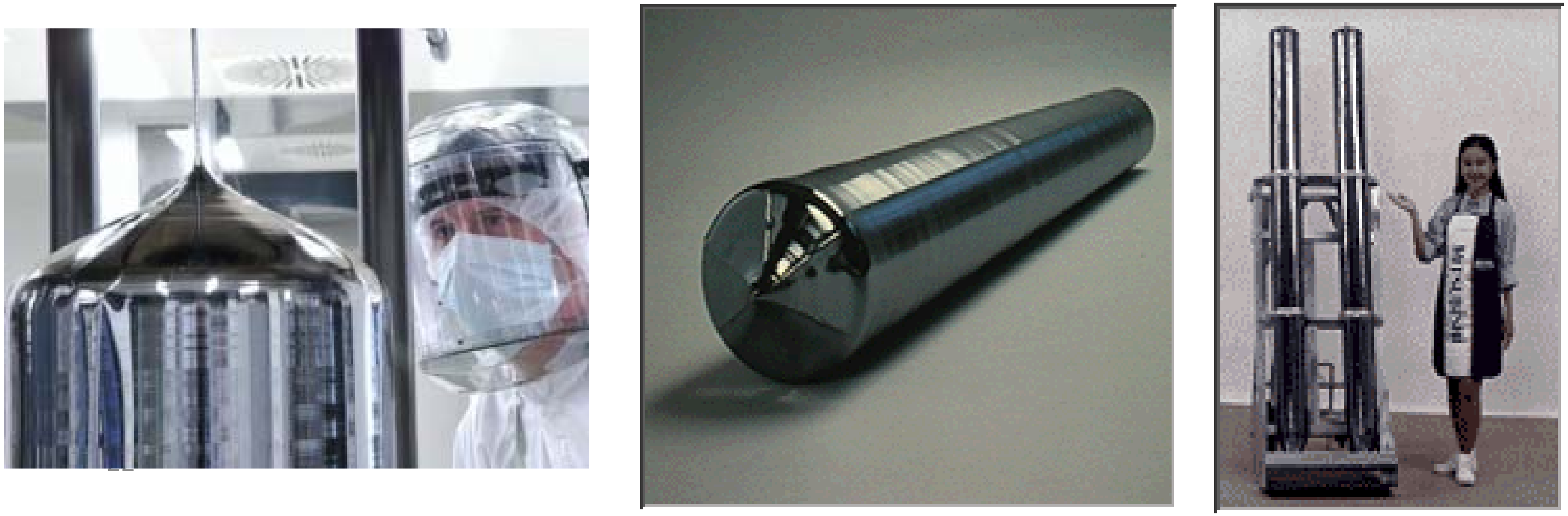
SENSOR FABRICATION

Sensor Fabrication (1)

1) Start with very pure quartzite sand (usually from an Australian beach or Sahara desert!), clean and further purify by chemical processes. Melt, and add the tiny concentration of phosphorus (boron) dopant to make n(p) type silicon (dopant concentration determines resistivity). Pour in mold to make a polycrystalline silicon cylinder.

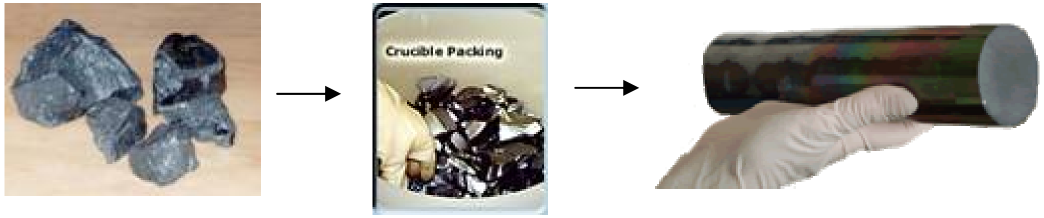
2) Using a single silicon crystal seed, …

3) Result is a single crystal of silicon (“ingot”)!



Sensor Fabrication (2a)

- A crystalline silicon growth method.



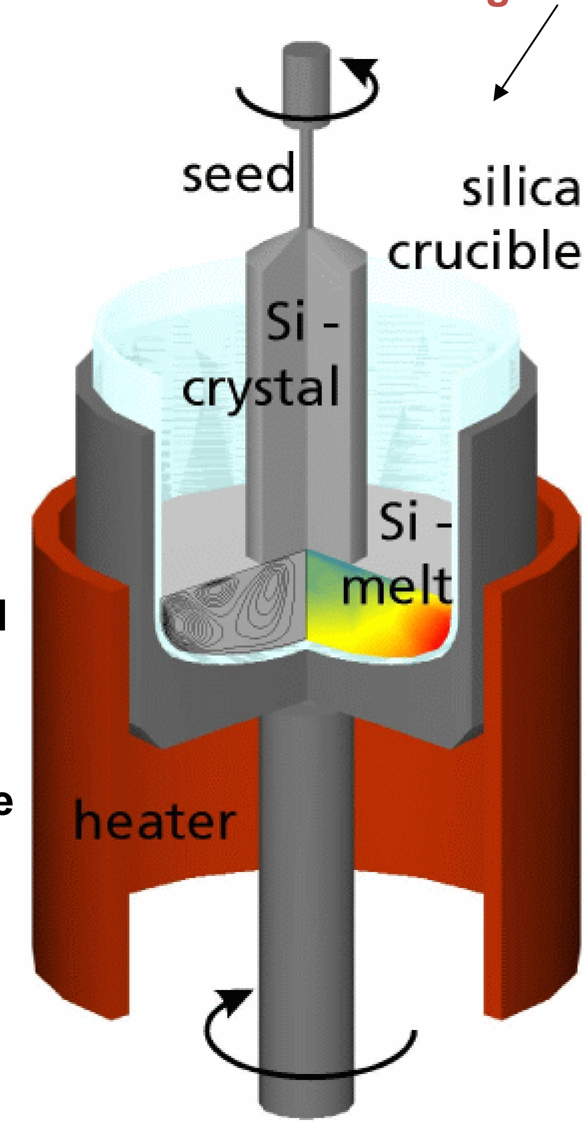
  - The growth method used by the IC industry.
  - Recent developments (~3 years) has meant that the Cz silicon is now of sufficient purity to allow use for HEP detectors.


Czochralski Growth

- **Cz Silicon has an intrinsically high level of oxygen.**
- **MCz is Cz silicon grown in the presence of an magnetic field.**
- **Cheap production..**

Czochralski Silicon

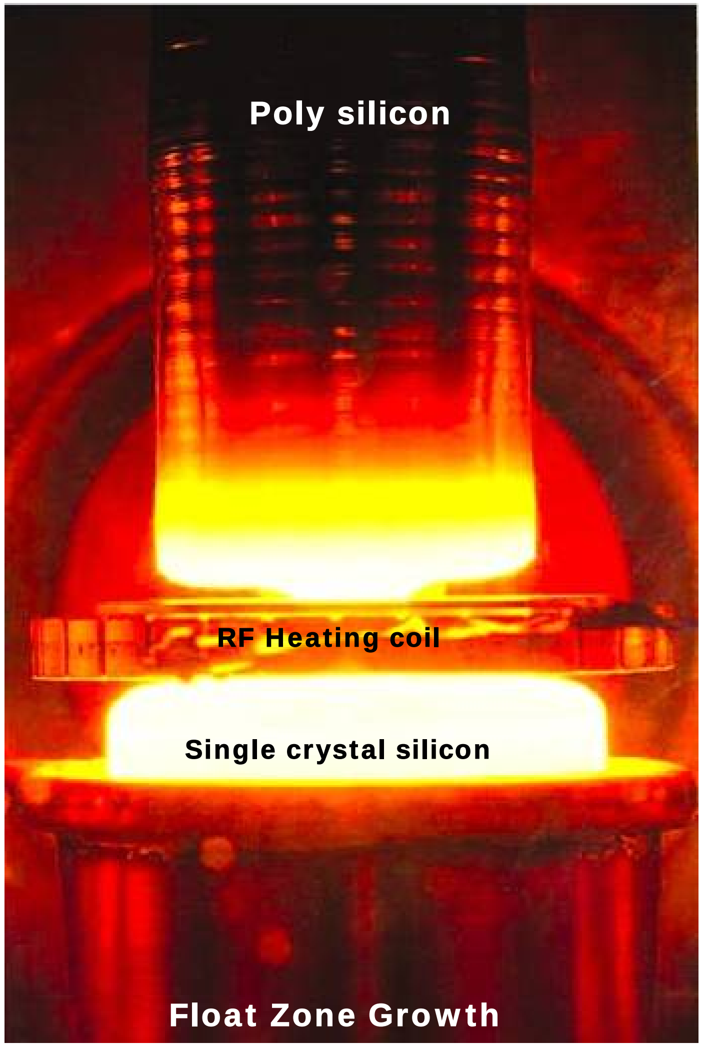
Pull Si-crystal from a Si-melt while rotating.



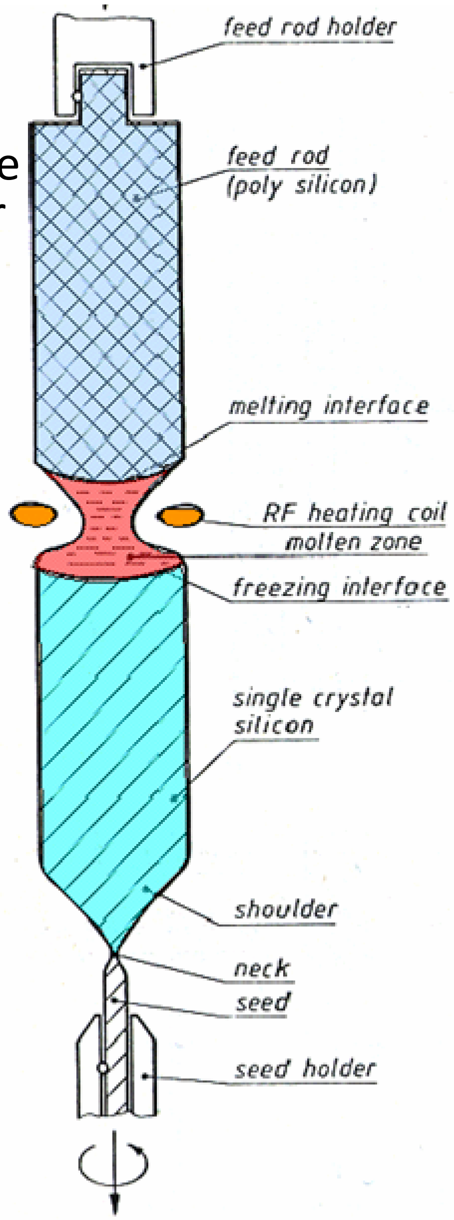
Sensor Fabrication (2b)

Float Zone silicon (FZ)

-the usual growth method used
to make HEP detectors



- Start with a polysilicon rod inside a chamber either in a vacuum or an inert gas
- An RF heating coil melts ≈2 cm zone in the rod
- The RF coil moves through the rod, moving the molten silicon region with it
- This melting purifies the silicon rod
- Oxygen can be diffused into the silicon – called Diffusion Oxygenated Float Zone (**DOFZ**) (done at the wafer level)



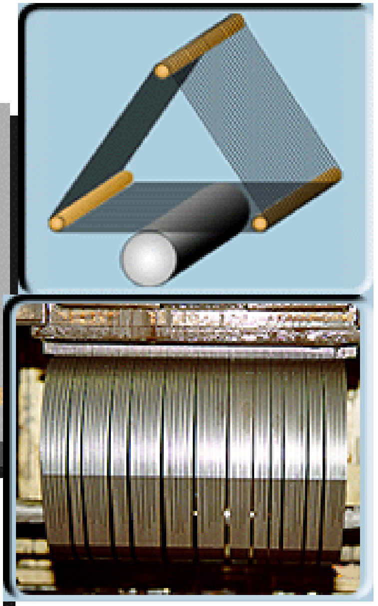
Sensor Fabrication (3)

- Slicing, lapping, etching and polishing

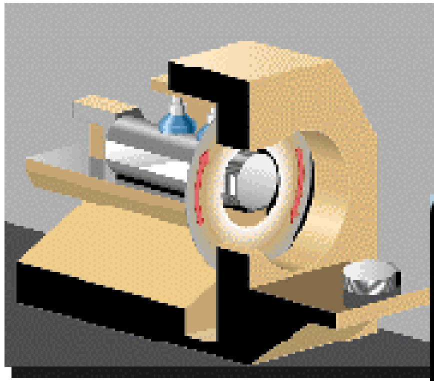
1) Ingot is sliced into wafers of thickness 300-500μm with diamond encrusted wire or disc saws.

2) Lapping (grinding away large imperfections), etching (more removal of impurities and imperfections), and polishing are needed to attain the desired wafer thickness and to ensure a surface with minimal defects.

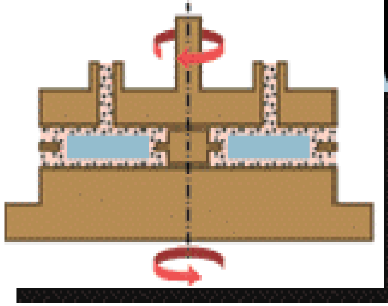
MWS



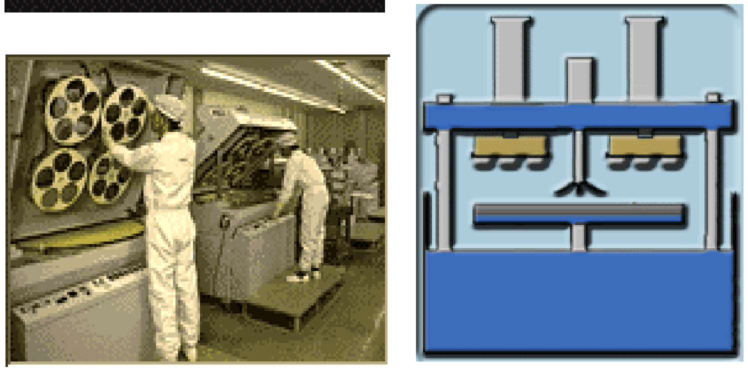
diamond disc saw



lapping machine

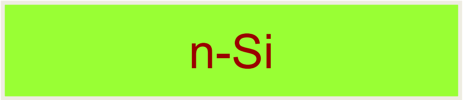


polishing machines

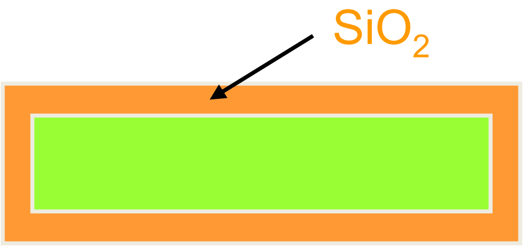


Sensor Fabrication (4)

- Wafer processing (1)

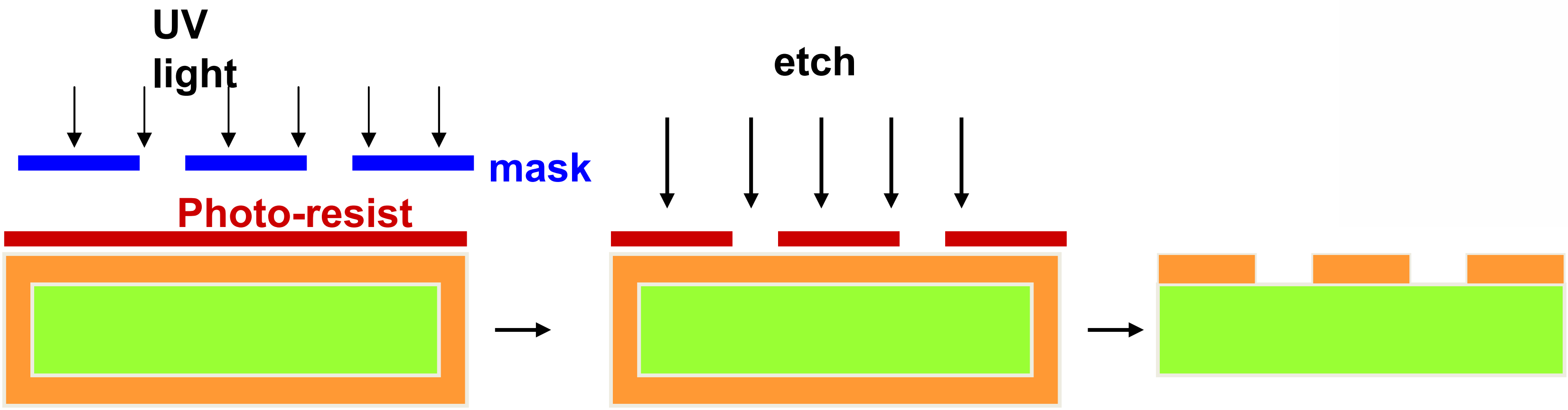
1) 

Start with n-doped silicon wafer,
ρ ≈ 1-10 kΩcm

2) 

Oxidation at 800 - 1200°C

3) Photolithography (= mask align + photo-resist layer + developi
followed by etching to make windows in oxide



In Fig. 1.39 both plasma and wet etching laboratories are shown. The full etching recipes are always adapted to the dedicated device and are an important know-how of the manufacturer. Basically Si is etched in a two-step process

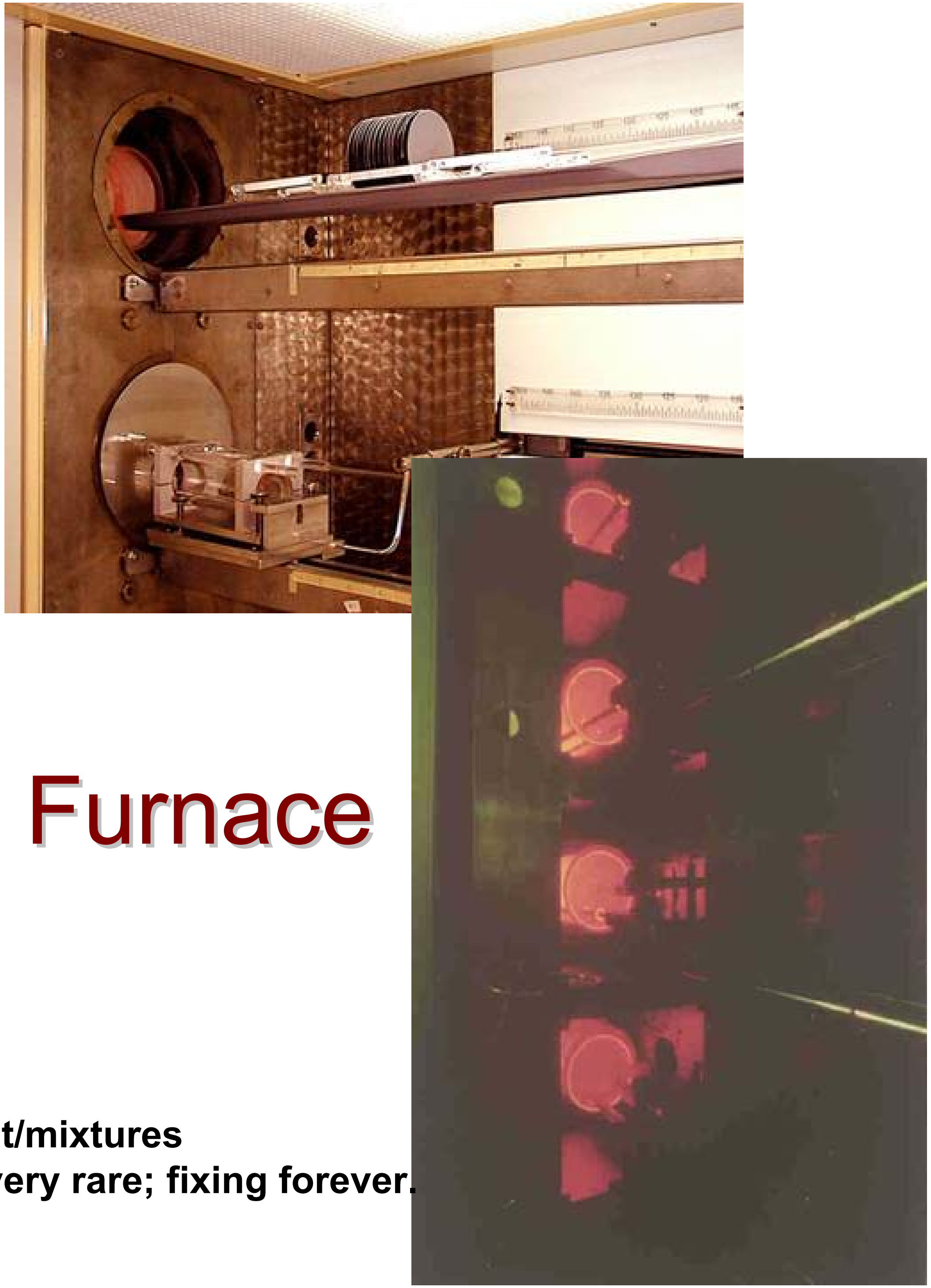
Oxidation $Si + 2HNO_3 \rightarrow SiO_2 + 2HNO_2$
Reduction $SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$

while etching of SiO_2 is a one step process

Etching $SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$

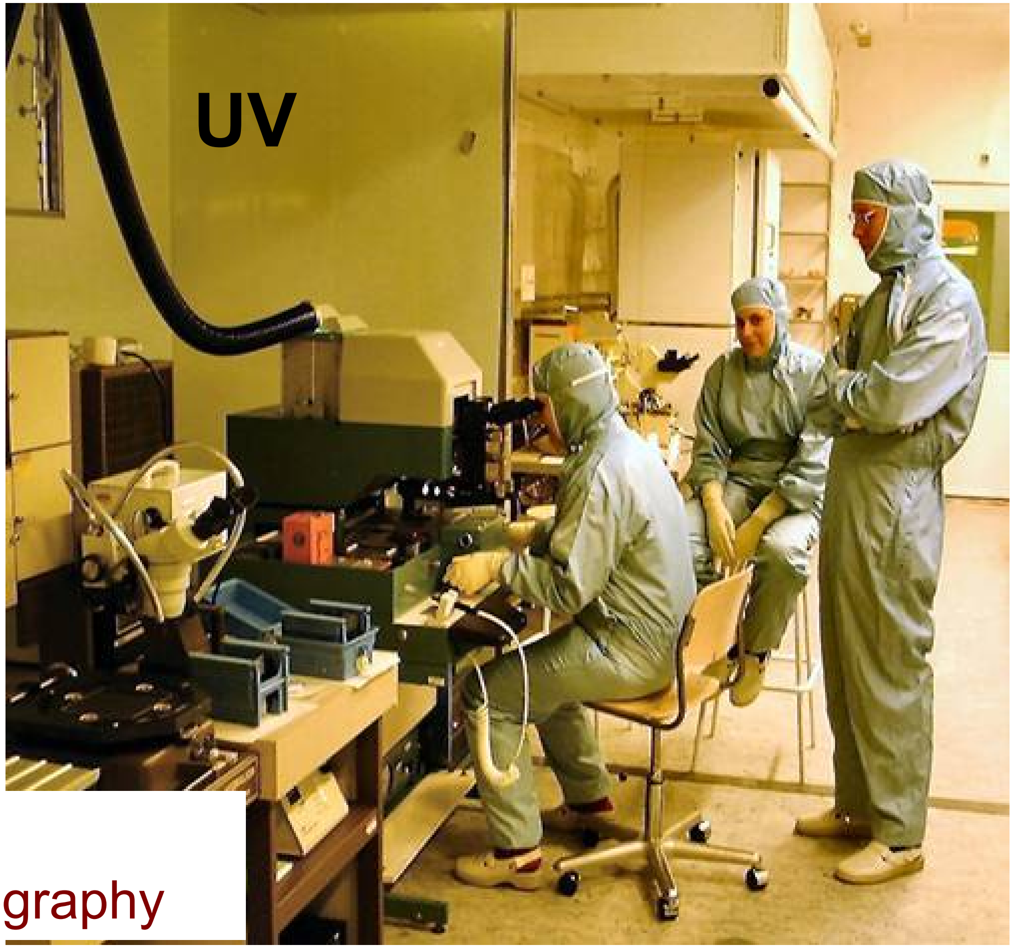
N.b.:
Clean, clean, always clean! Clean more!

Furnace



One furnace per element/mixtures
Changes even in T are very rare; fixing forever.

Sequence in a nutshell:
Wafer insertion ➔ guiding ➔ cleaning/etching
➔ photoresist drops while wafer is spinning
➔ heating ➔ cleaning ➔ output
➔Mask alignment➔UV
➔develop



Alignment ➔ UV

Remember:
Each processing step requires lithography

Photoresist Spinning (Cover Wafer)

Fig. 1.37 Photoresist is roughly spilled in the middle of the wafer, centrifugal forces, during fast rotation, homogeneously distributes the resist on the wafer. Courtesy of ITE Warsaw [156]

Plasma etching

(directive etching)

N.b.: There is a special etching recipe for each material; e.g. Si, SiO2; Al, ..
(one of the many company secrets)

Etching time well known!

Wet etching

During plasma etching X-Rays are damaging the structure ➔ post-annealing is necessary

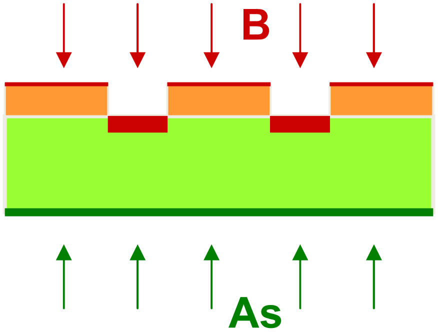
➔ Final Al processing mostly done with wet etching

Q: which process do you use for process X at step Y?
A: I’m sorry, that’s a company secret; but don’t worry it only takes you some years to find out.

Sensor Fabrication (5)

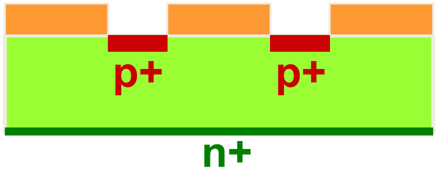
- Wafer processing (2)

4)



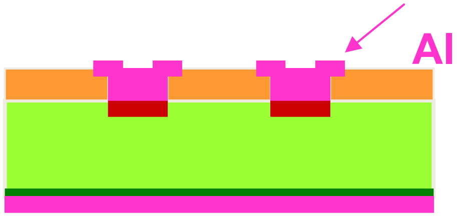
Doping by ion implantation (or by diffusion)

5)

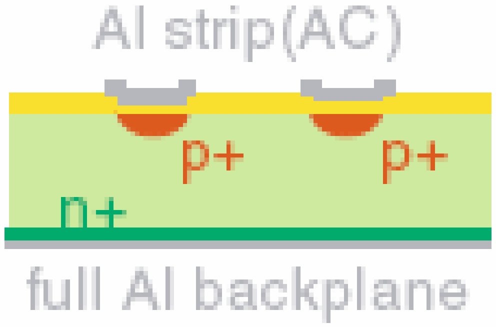


Annealing (healing of crystal lattice) at 600 °C

6)

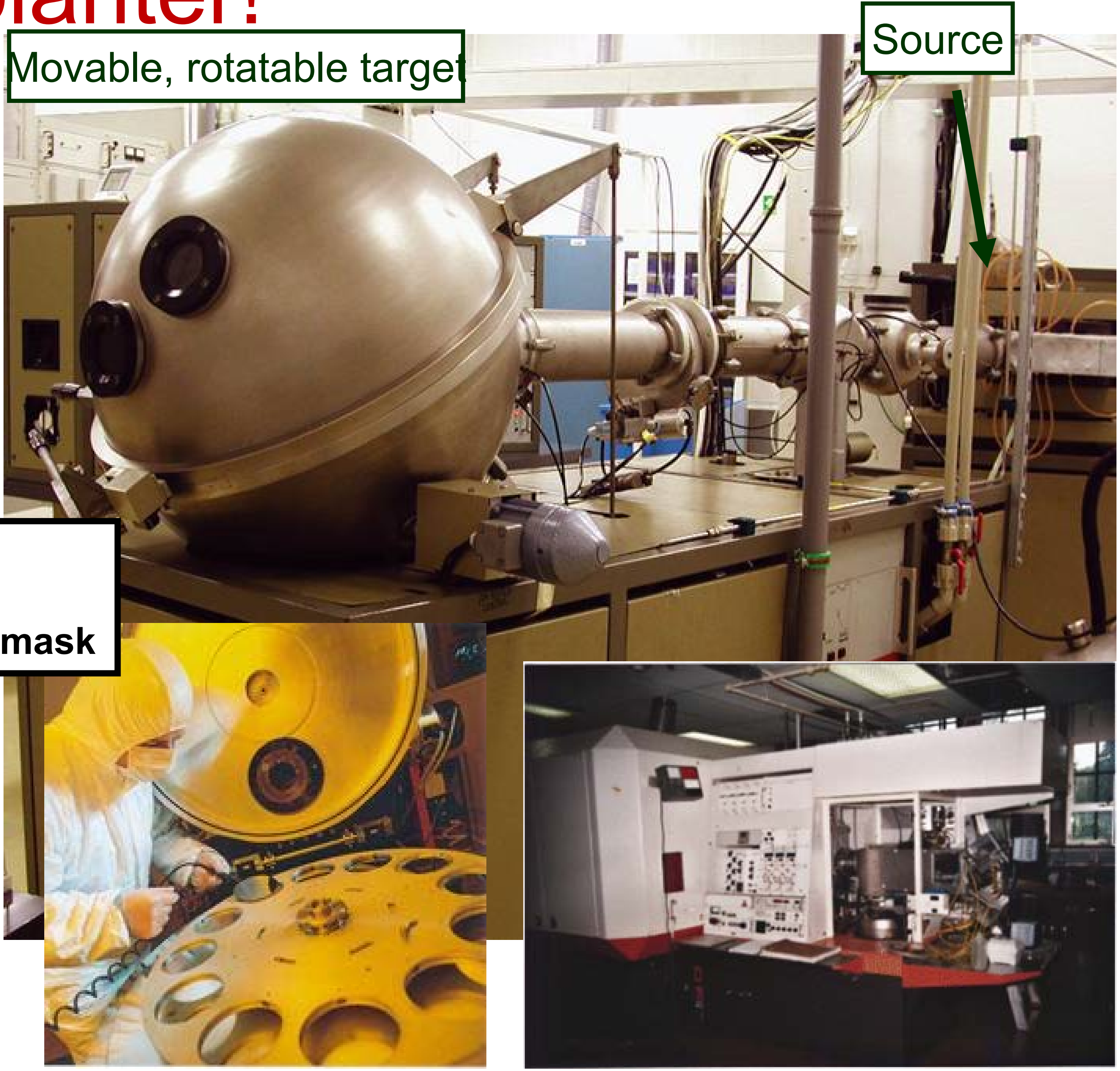


Photolithography followed by Al metallization over implanted strips and over backplane usually by evaporation (CVD)



- *Most simple DC-coupled silicon strip detector*
- *More often an additional SiO2 layer is grown, before the metallization*
- *Sometimes both faces are structured (double sided sensor)*
  - *This needs several additional steps (and a special strip isolation)*

Ion implanter!



Remember:
Uniform irradiation!
Features defined by mask

One strip

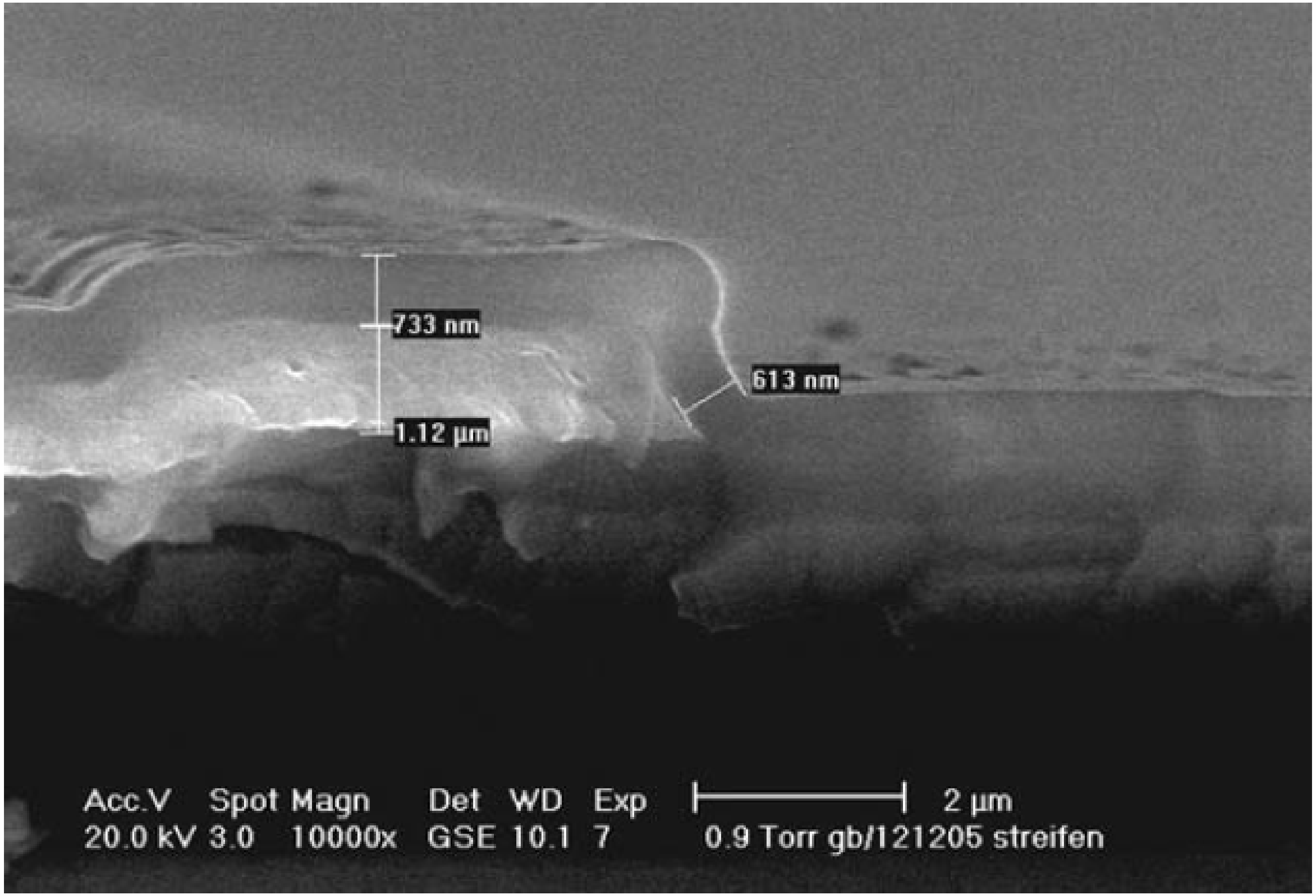


Fig. 1.25 Cut perpendicular through a single strip. The picture shows the upper part, especially the metal part and the passivation oxide protecting it from the environment

Sensor fabrication (6)

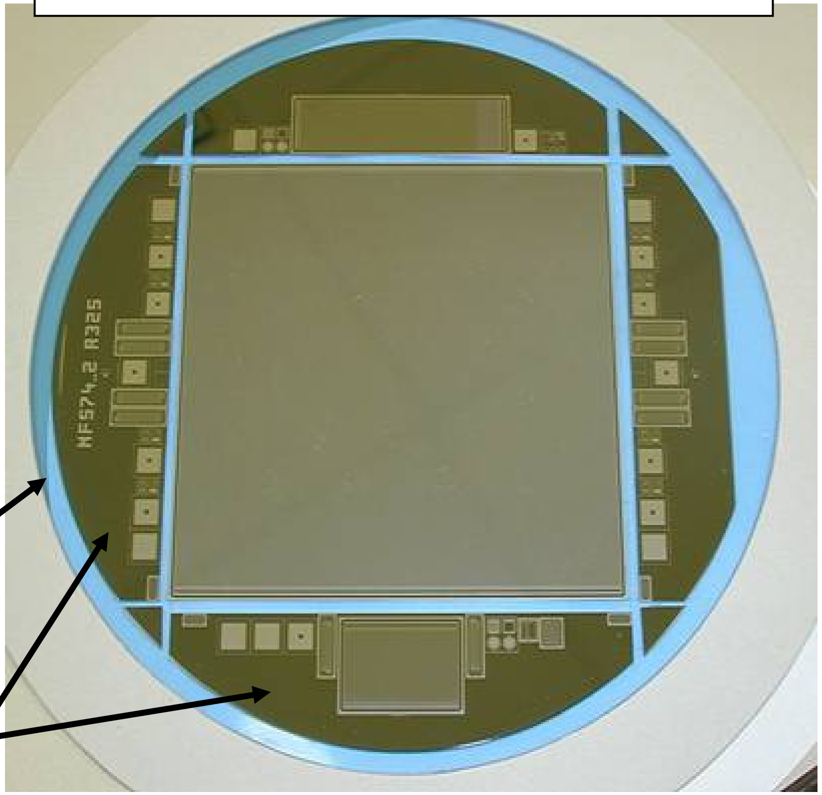
- Wafer processing: Passivation
  - Passivation is the application of a layer of SiO_2 or other suitable material (polyimide is very common) to protect the surfaces not needing to be electrically contacted from physical damage, chemical interactions, and other environmental effects (humidity).
- Wafer processing: Cleaning
  - A cleaning step is *usually* performed to remove any residual chemicals left from the processing steps.
- Wafer processing: Testing
  - In general device testing is then performed in order to see the quality of the devices on the wafer. This is often done prior to cutting out the individual devices.
  - Test structures are often included on the wafer design in order to test specific properties of the processing and design (see next slide).

Sensor Fabrication (7)

Wafer processing: Dicing

- Individual sensors are usually cut from the wafer using a diamond disc saw. Width of cut is about 50 microns.
- A "scribe and break" method has also been used.

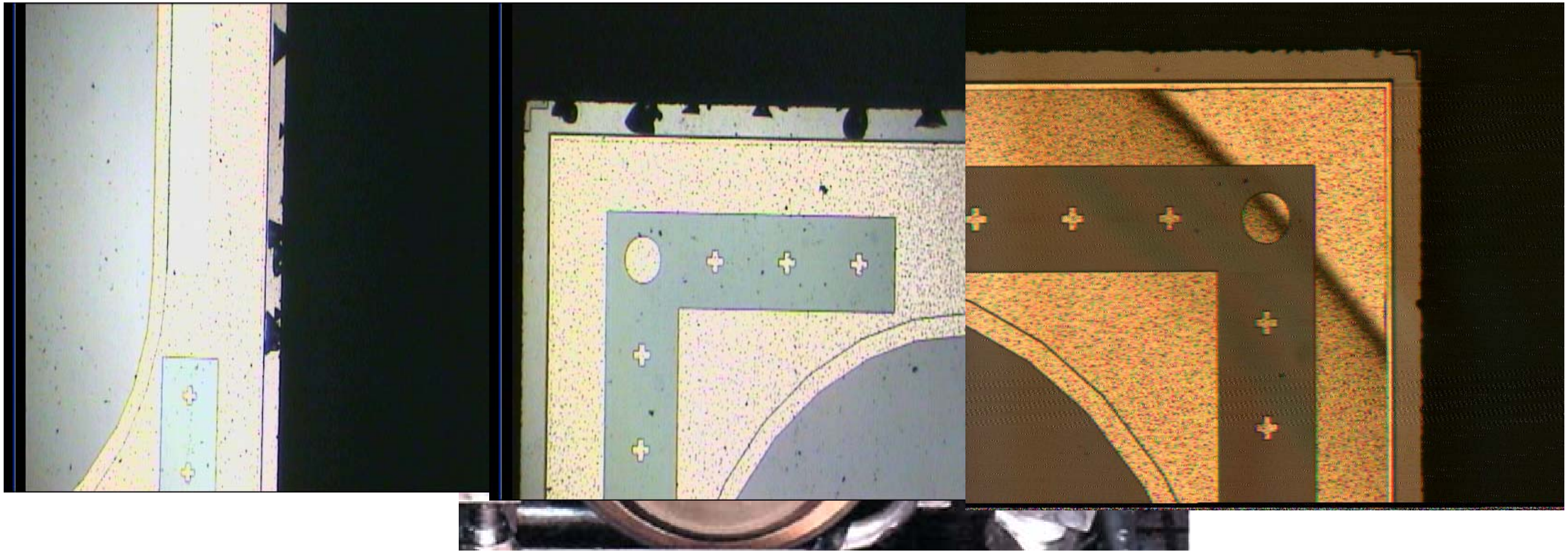
CMS silicon strip sensor from 6" wafer



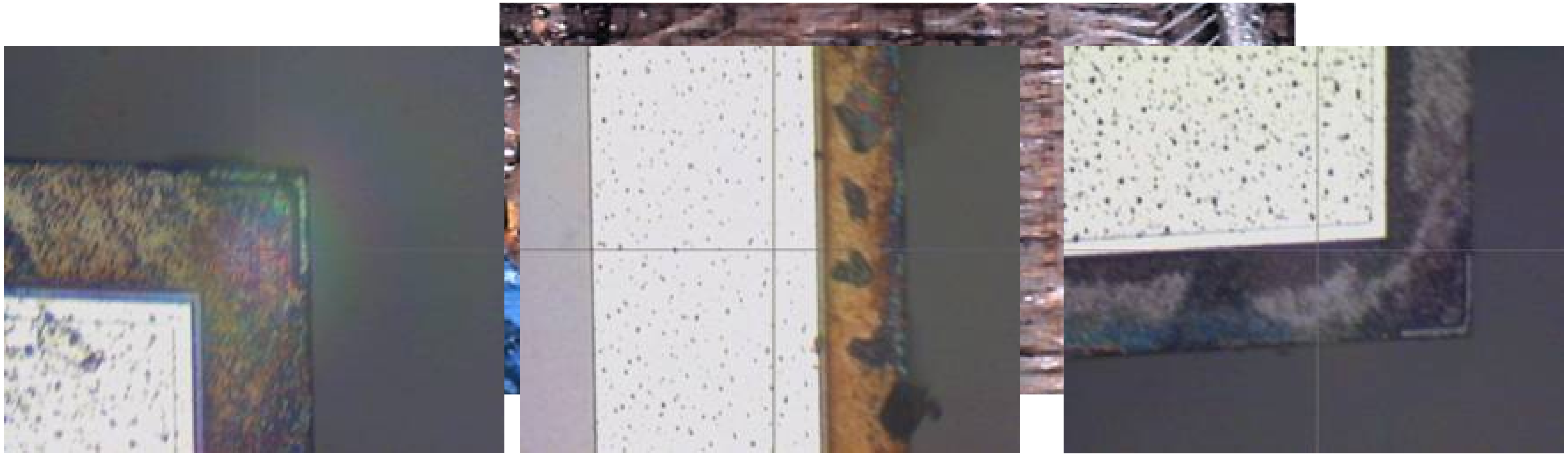
The wafer rests on a blue adhesive film

Test structures

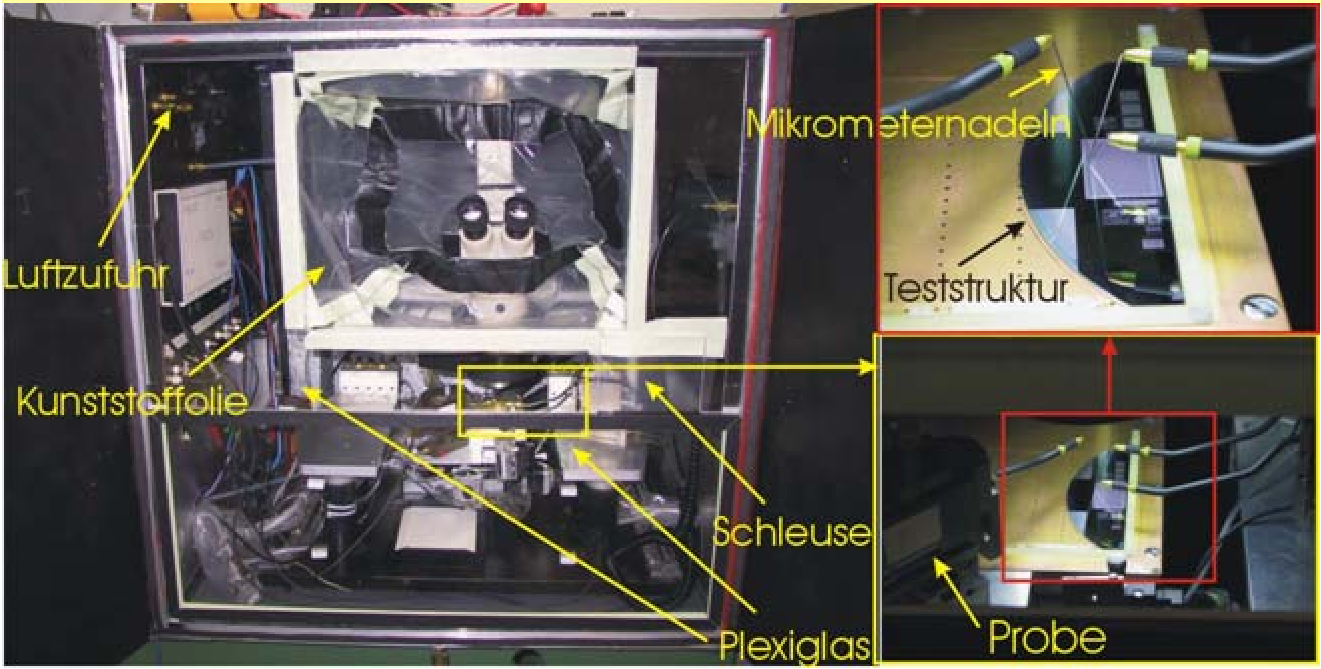
⇒ Sensors ready to be packed and shipped. Not without danger: I have seen in many instances destroyed sensors after shipping!



Maybe not!



Testing at the Universities



2 homemade flexible probestations

- 6”
- cold chuck -10°C (+100°C to -10°C)
- very flexible
  - individual needles
  - bias travels with sensor
- switching matrix
- RH control
- LCR, electrometer, HV, quasistatic CV!
- Camera (incl. frame grabber)

Measurements (all implemented):

- Global: IV,CV
- Strip:
  - current, CaC, diel current
  - interstrip cap, resistance
- Special: VFlat, Isurf
- All paramaters vs. time

Suitable for strip characterization of sensors and full modules

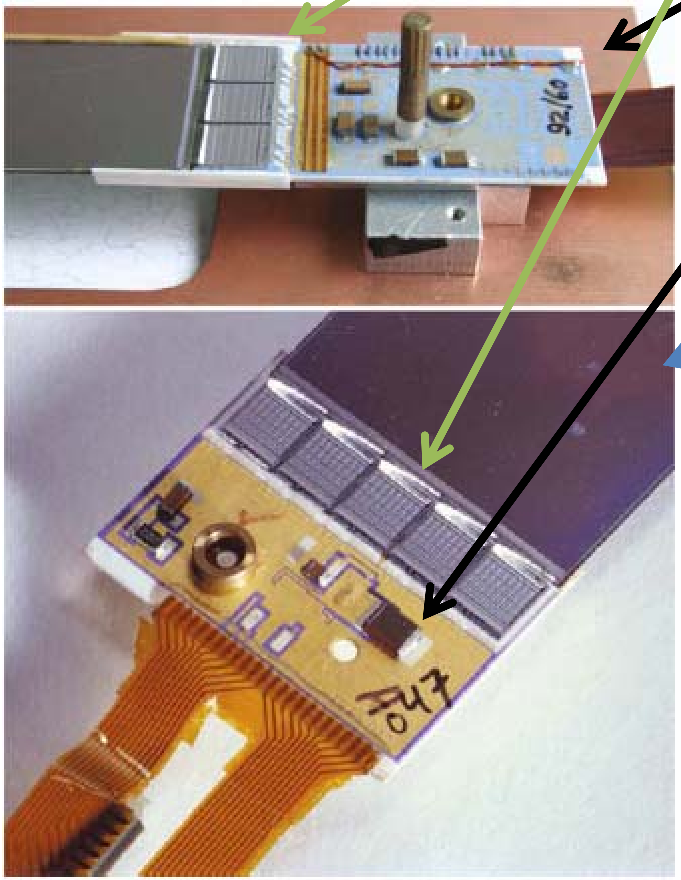
MODULES AND LARGER STRUCTURES & SOME VARIETY EXAMPLES

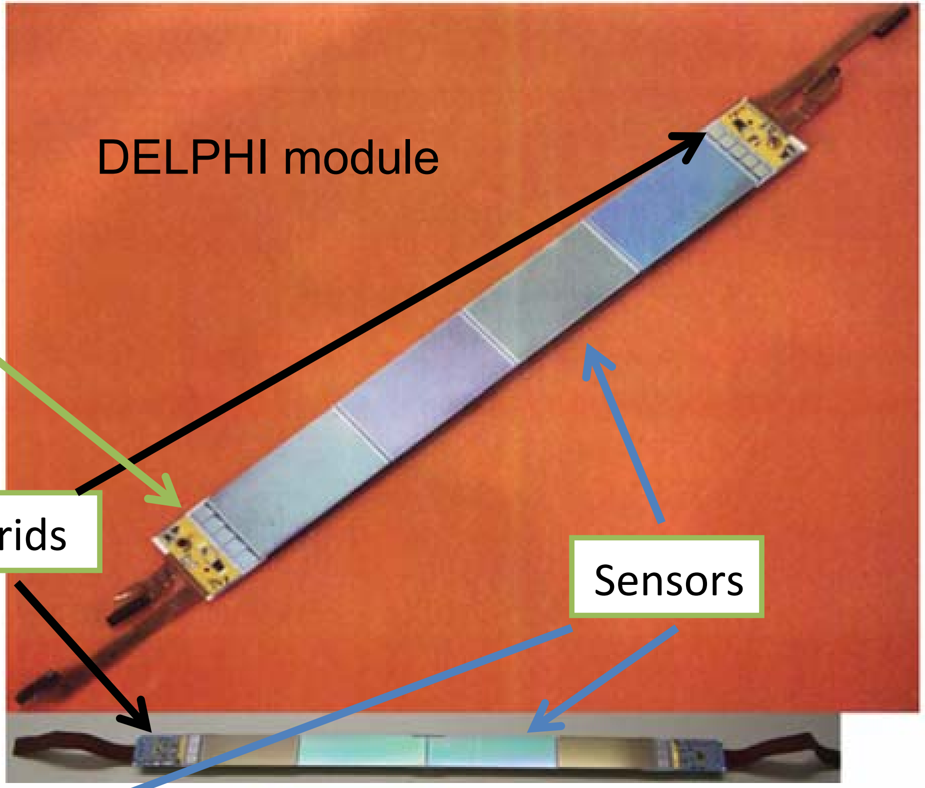
From a Sensor to a Full Module

Chips

Hybrids

Sensors





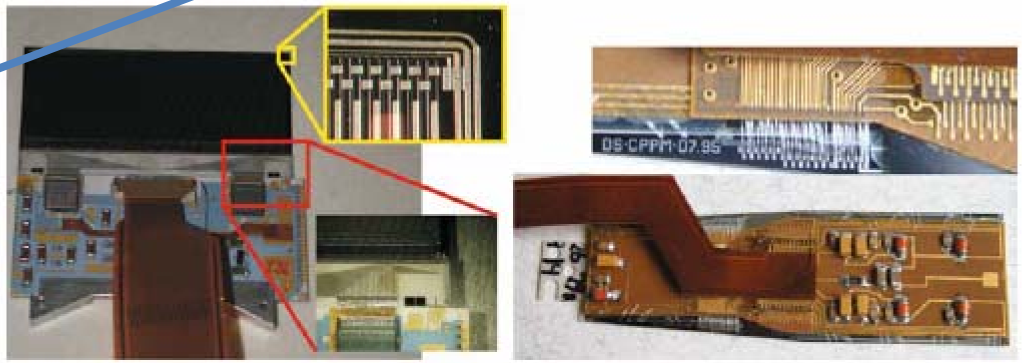


Fig. 3.9 A DELPHI ministrip and pixel module. The *left* picture shows one side of a Ministrip sensor module. The hybrid to sensor wire-bonding happened in the middle of the sensor. The sensor itself is biased via FOXFET. The FOXFET ring layout is shown in the exploded view of the sensor corner, the guard ring was connected to ground. A second zoom shows the hybrid edge including the chip edge. Two chips are sufficient for the 256 strips. The *right* picture shows a complete pixel module. The sensor-chip sandwich (bump-bonded) is covered by a Kapton flex structure carrying the necessary passive components and the bus lines. The exploded view shows the wire-bonding from pixel chip bus lines to Kapton bus lines [103]

Chips & Modules (A lecture in its own)

- Don‘t forget, most of the electronics are dedicated and home designed!
  - All experiments use dedicated chips and drivers
    - Time constants, radiation environment, magnetic field have to be taken into account at the time of design
    - Capacities, currents, voltages, …

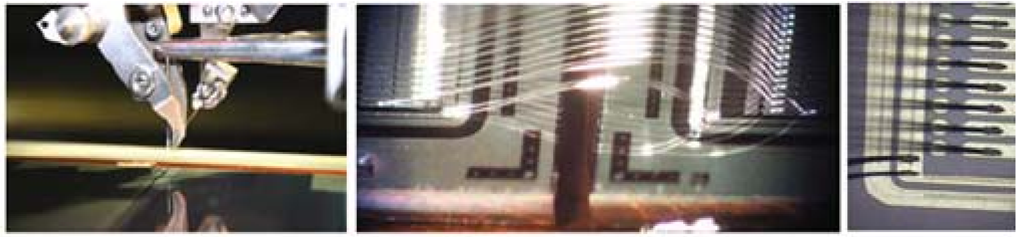
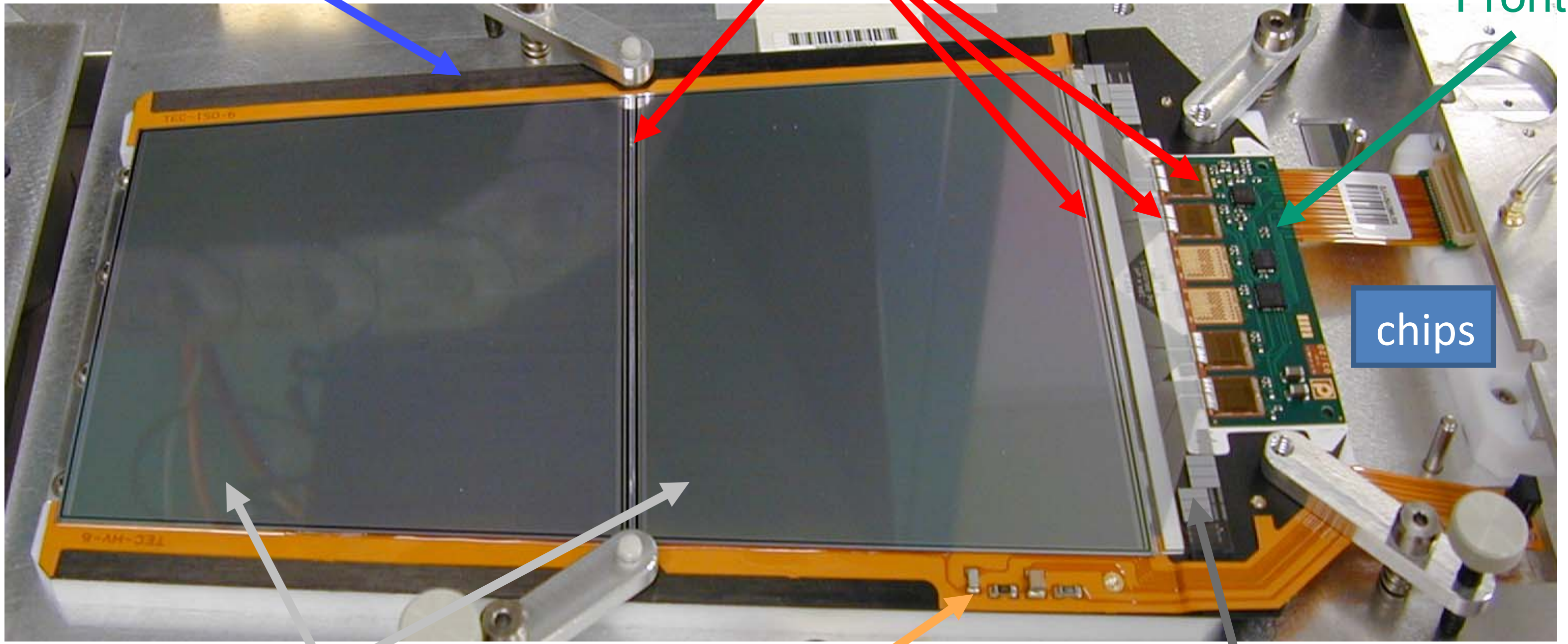


Fig. 5.24 CMS module bonding



Frame of carbon fiber

Micro-bonding

Front-end hybrid

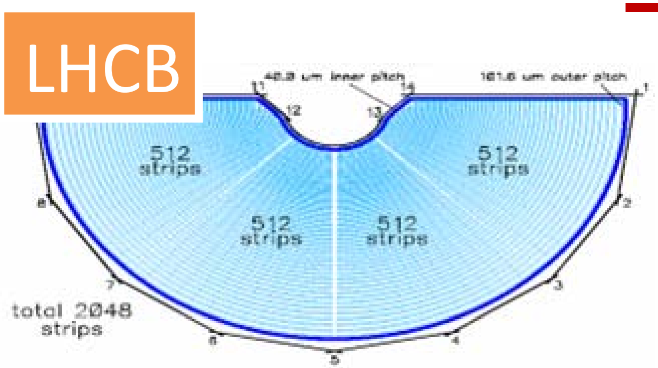
chips

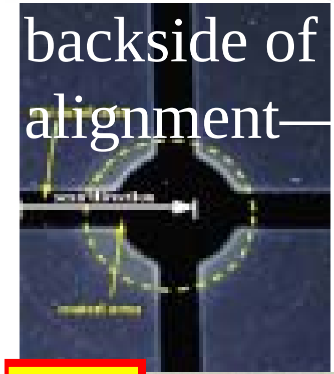
Sensors

Kapton & filter circuit

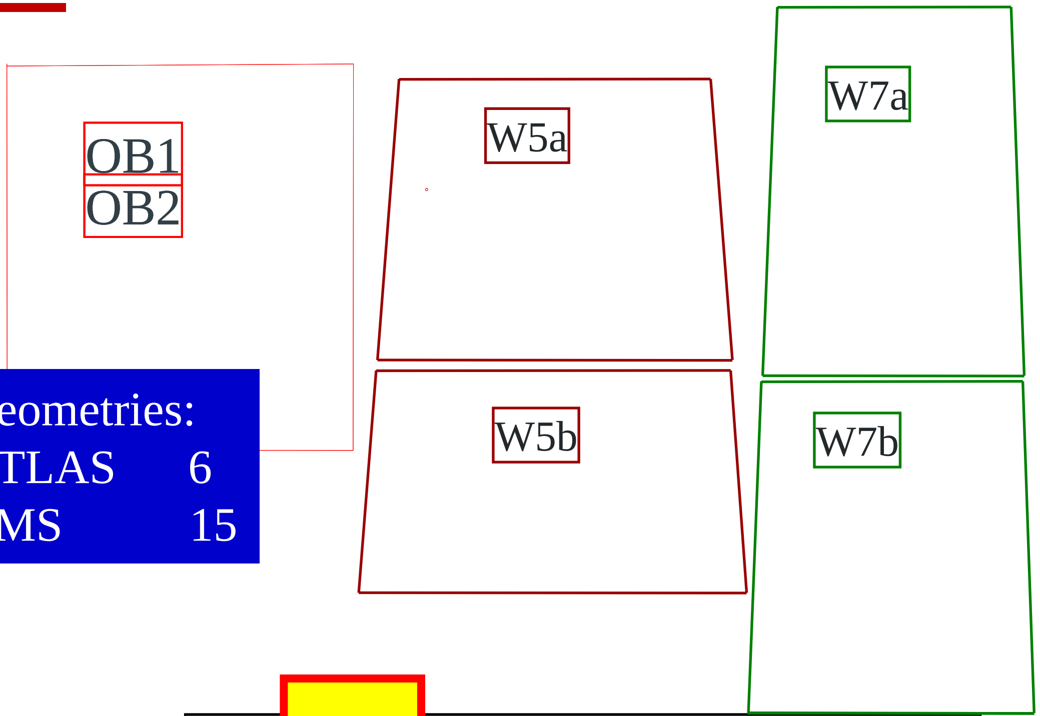
Pitch adapter (glass)

How does **THE** LHC sensor look like??





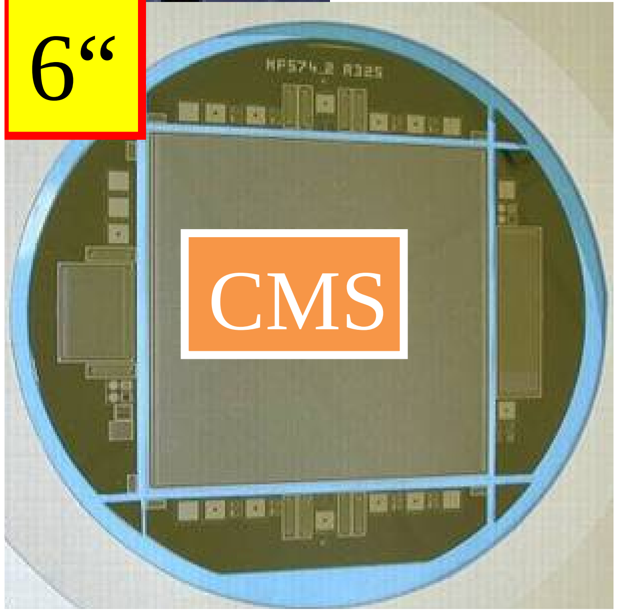
backside of the CMS alignment— Sensors

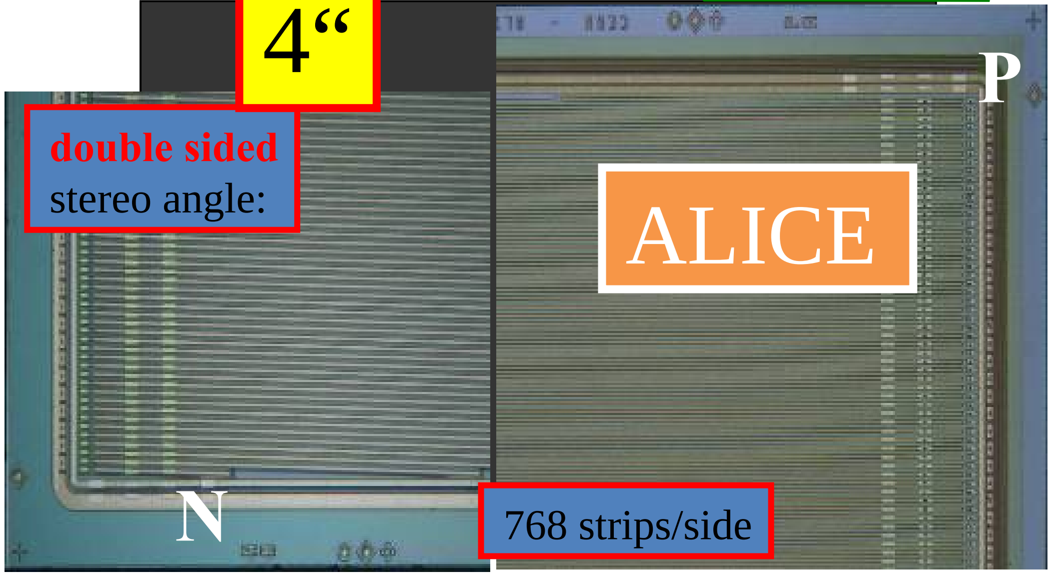


Geometries:

ATLAS	6
CMS	15

etc.





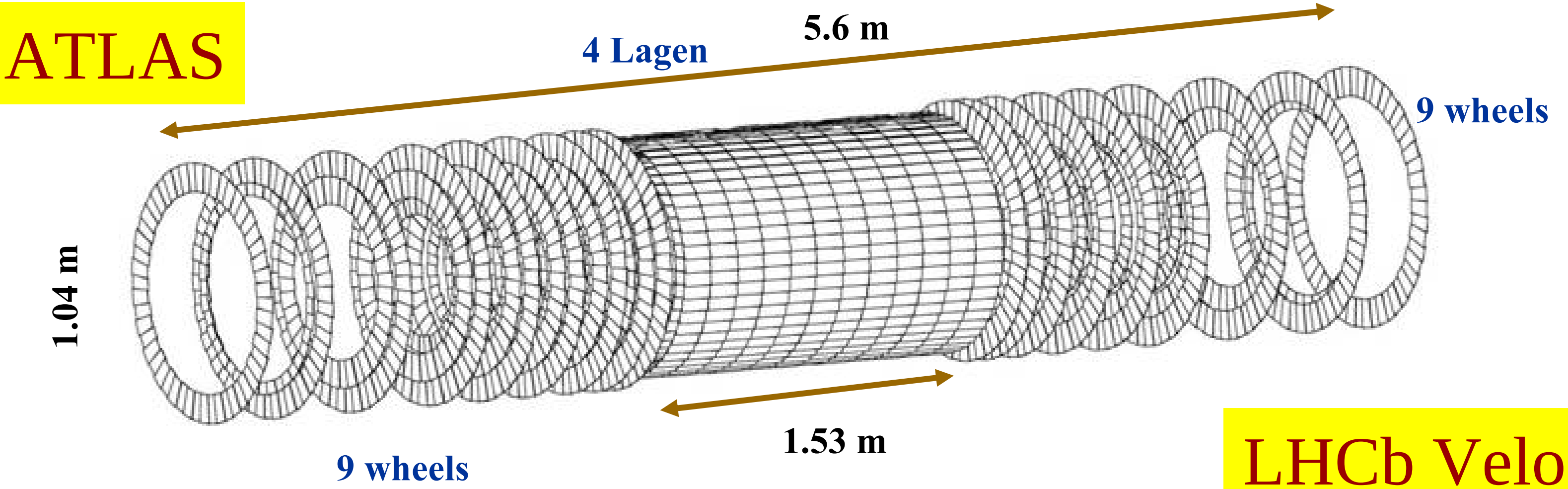
double sided
stereo angle:

768 strips/side

Source: ALICE Bregant Vertex ,05

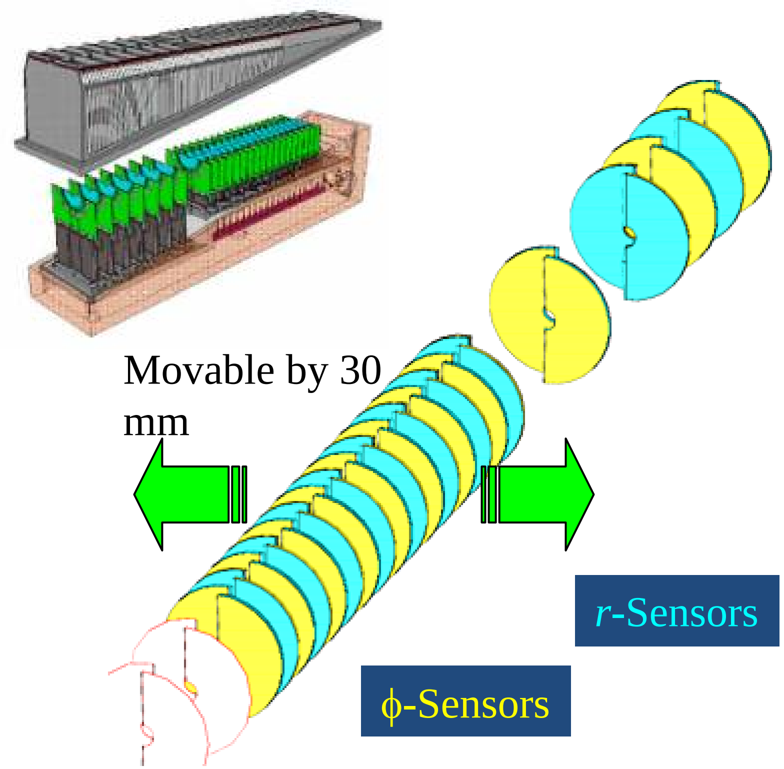
What is **THE** geometry of a tracking device?

ATLAS



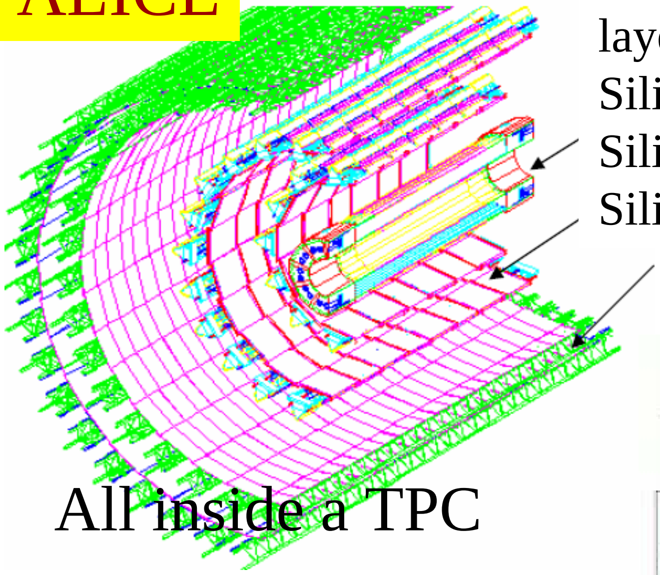
LHCb Velo

- Design



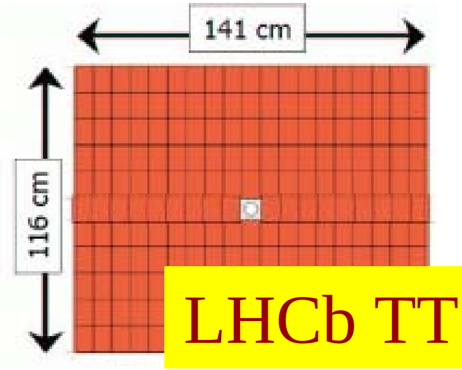
Movable by 30 mm

ALICE



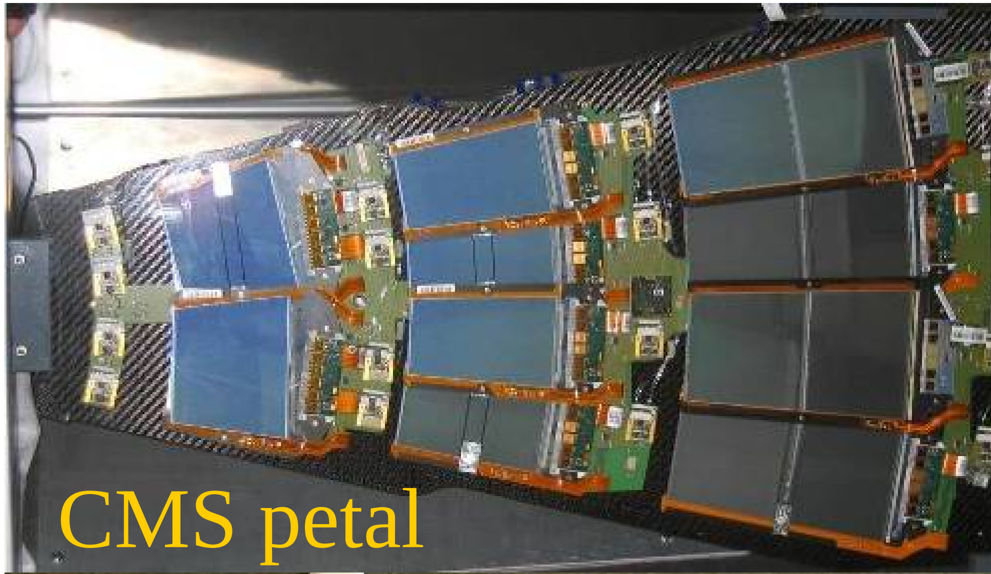
layers of
Silicon pixel
Silicon drift
Silicon strips

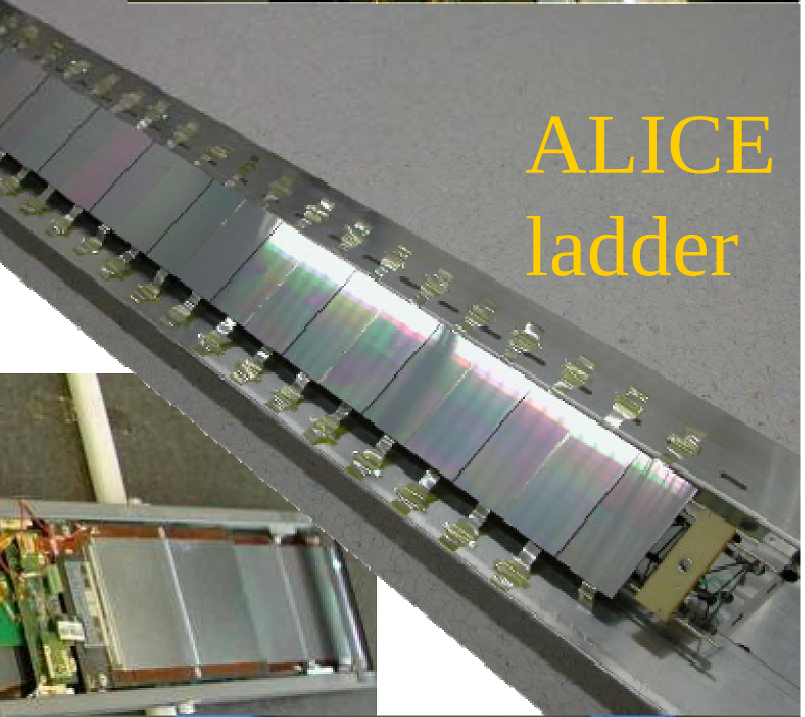
All inside a TPC

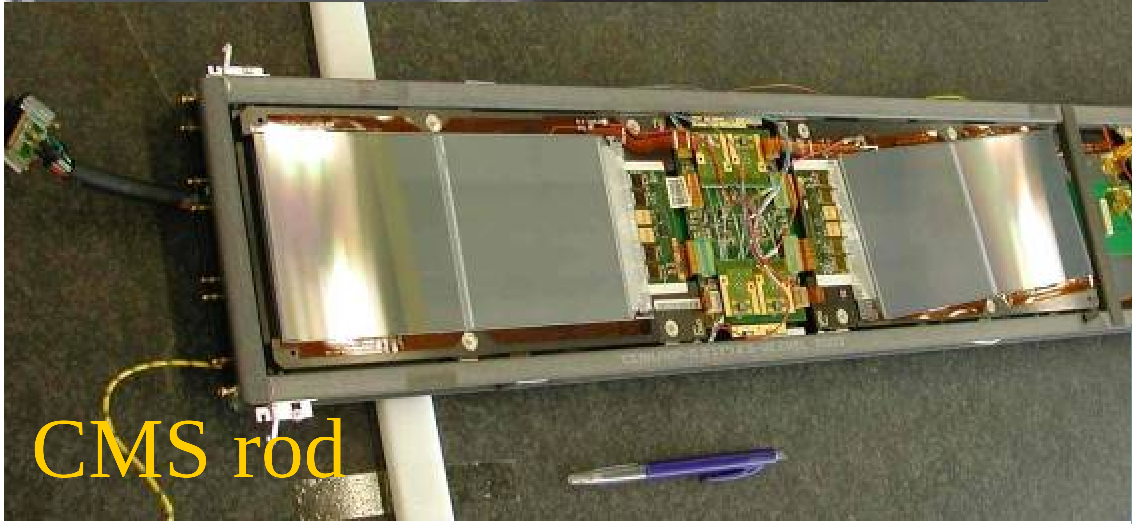


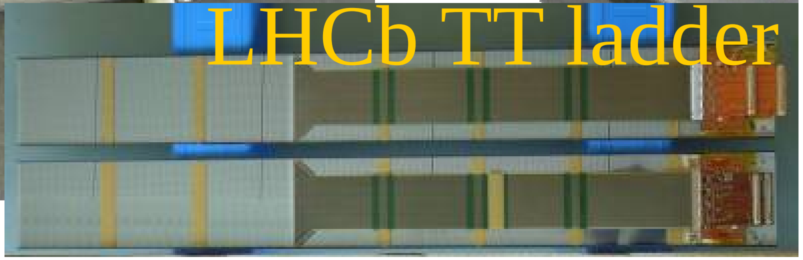
LHCb TT

Petals & rods & ladders & halfshells



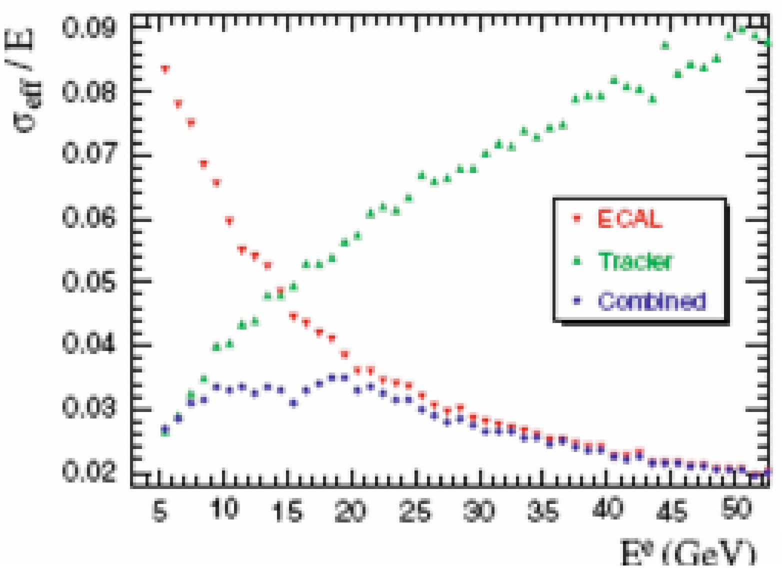






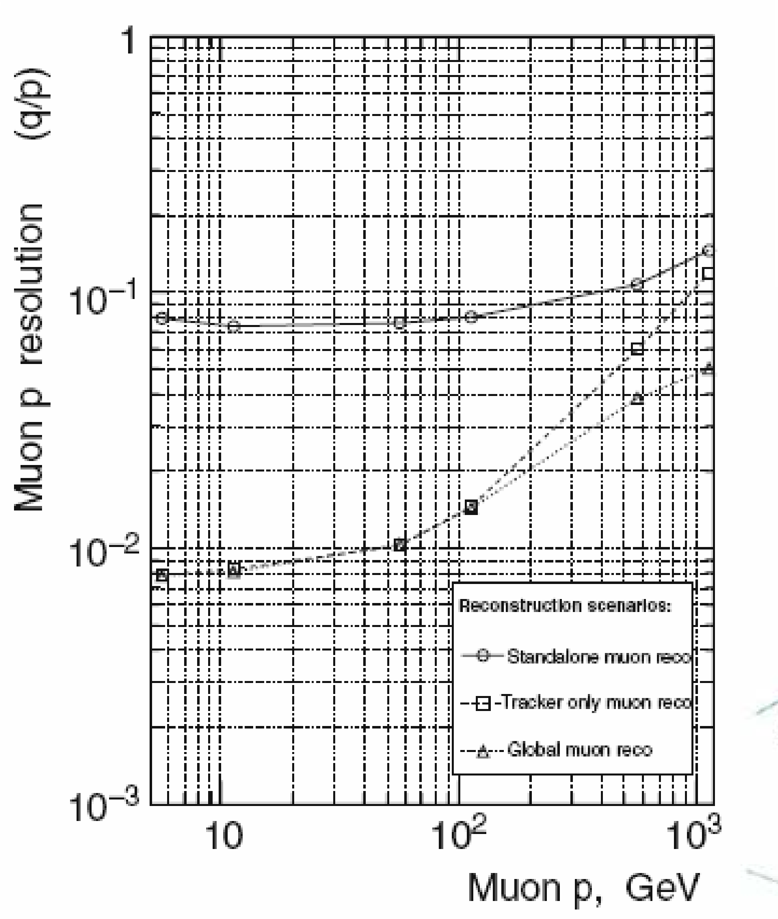
Up to 14 sensors per ladder(4 sensoren per hybrid)

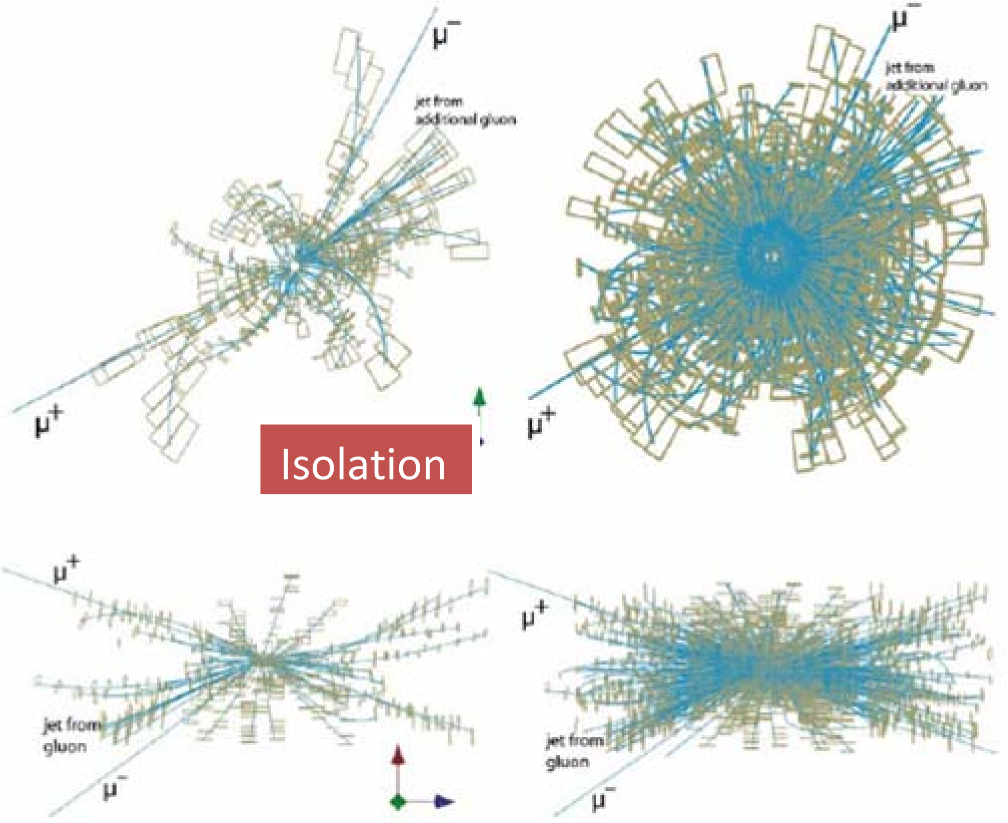
Is it useful for physics?



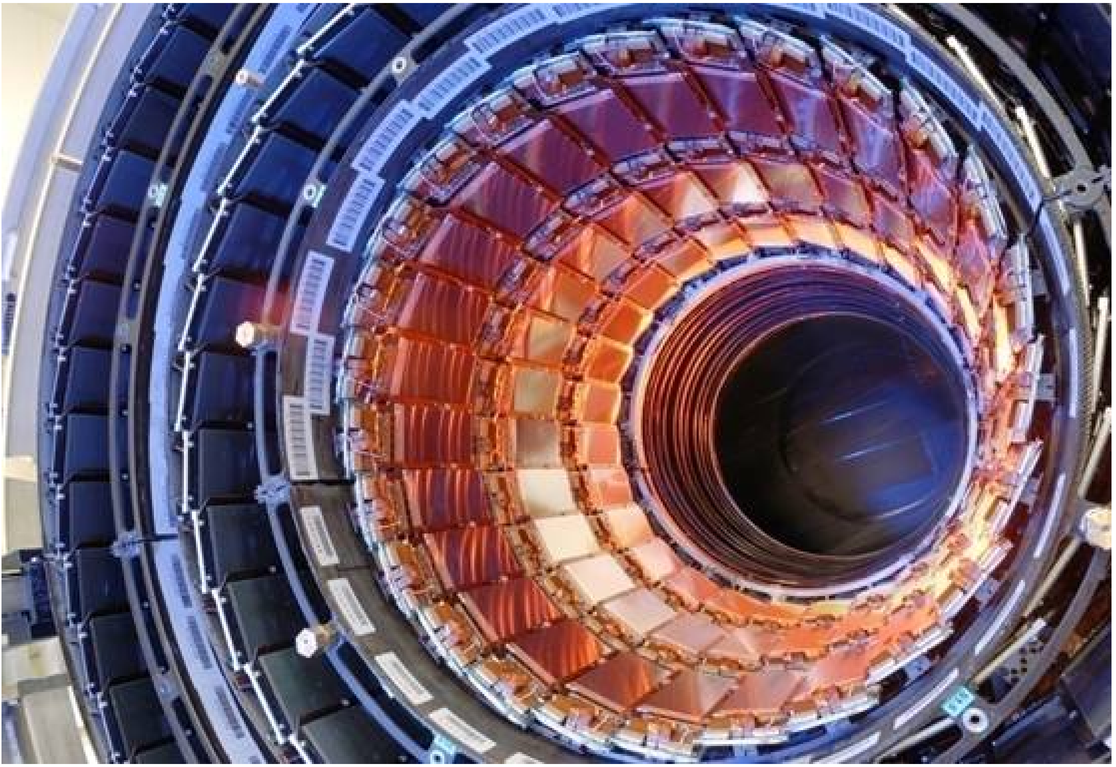
Energy measurement

Momentum measurement





Isolation



Strips: 206 m^2 area

25.000 silicon sensors

10Mio strips ≡ electronic channels

75.376 readout chips

26.000.000 bonds

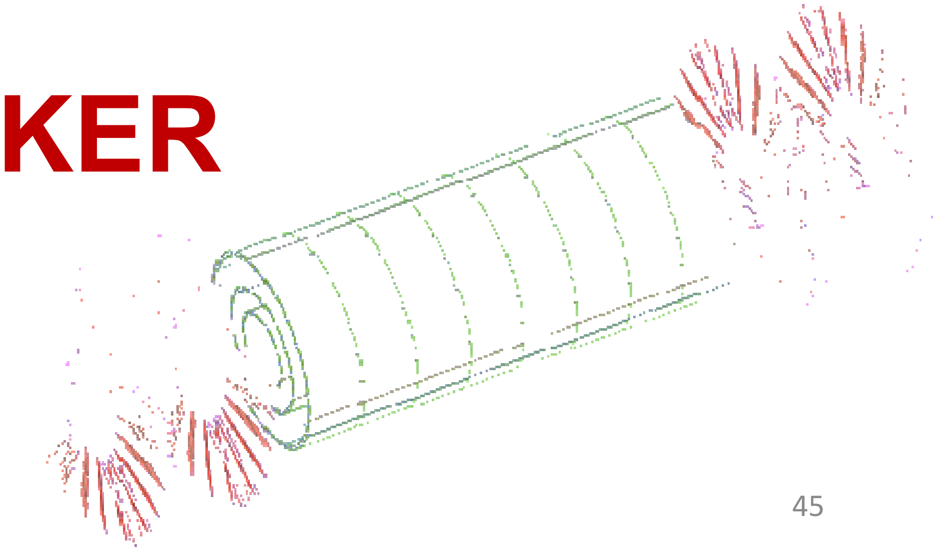
37.000 analog optical links

3.000 km optical fibers

Pixel: m^2 area:

66 Mio channels

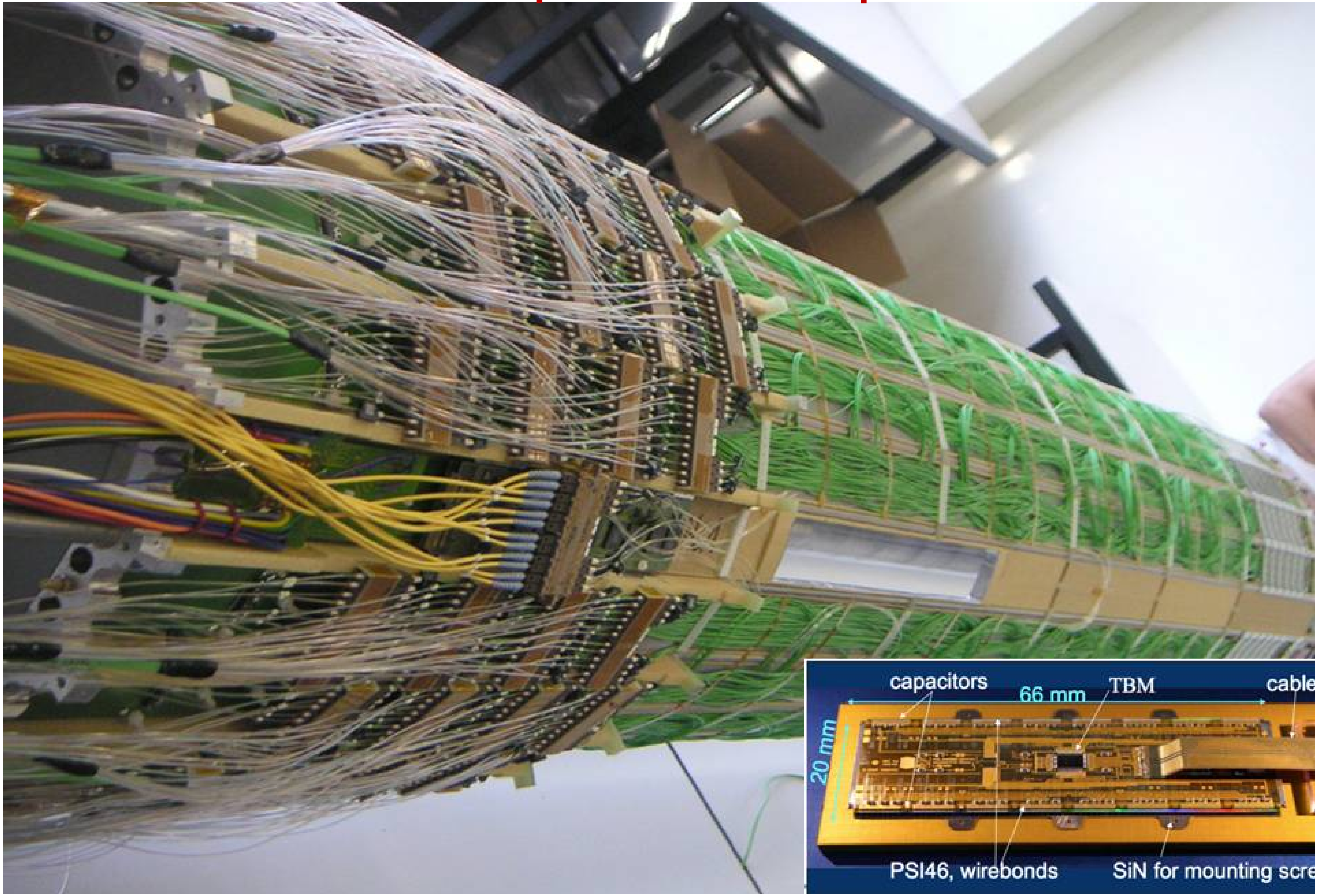
THE CMS TRACKER



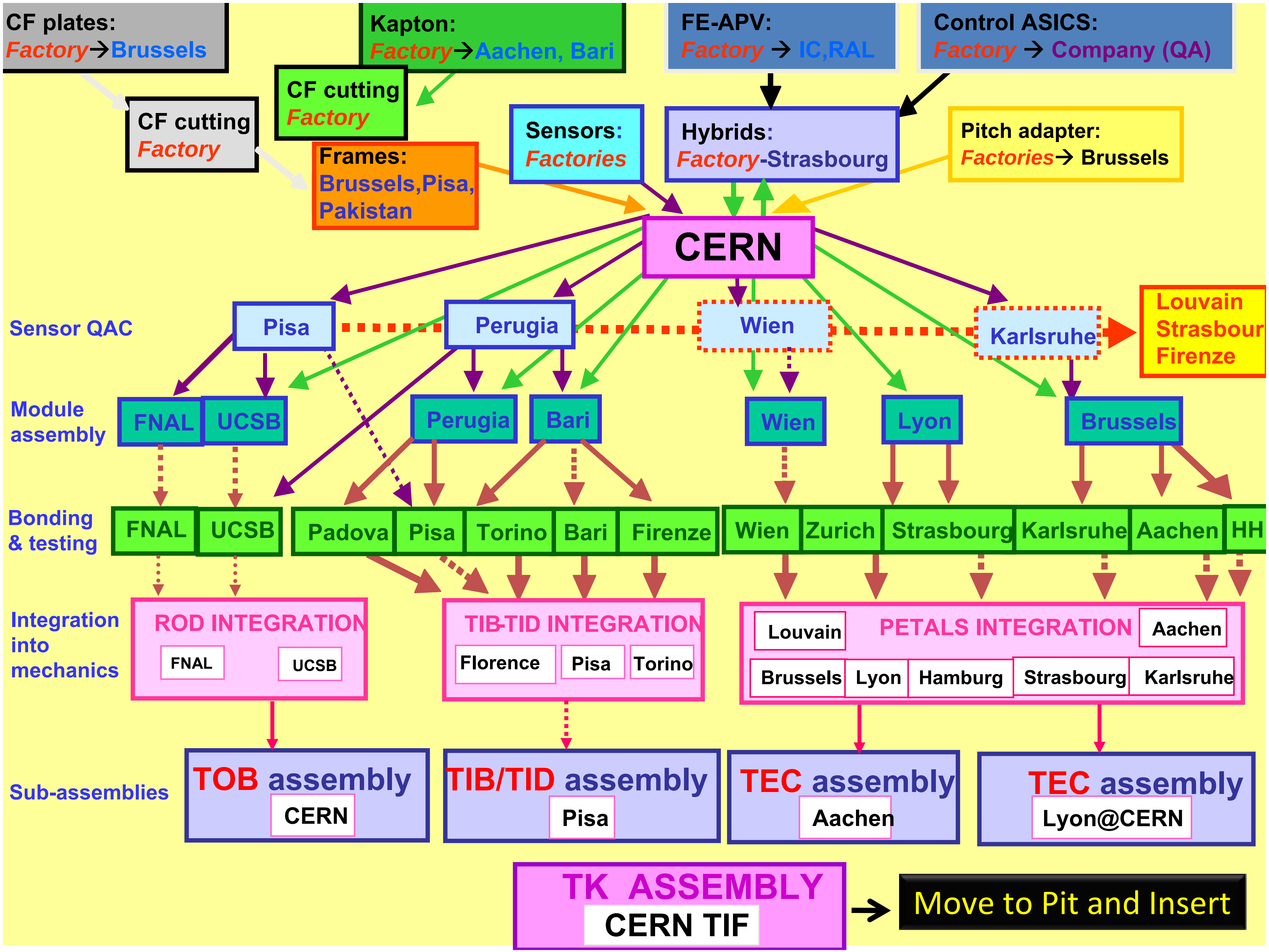
Half Disc of Forward Pixels

Forward Pixel: 672 plaquettes required

Pixel Barrel plus Endcaps READY



STRIP TRACKER



CF plates: Factory→Brussels

Kapton: Factory→Aachen, Bari

FE-APV: Factory → IC,RAL

Control ASICS: Factory → Company (QA)

CF cutting Factory

CF cutting Factory

Frames: Brussels,Pisa, Pakistan

Sensors: Factories

Hybrids: Factory-Strasbourg

Pitch adapter: Factories→ Brussels

CERN

Sensor QAC: Pisa, Perugia, Wien, Karlsruhe

Louvain
Strasbour
Firenze

Module assembly: FNAL, UCSB, Perugia, Bari, Wien, Lyon, Brussels

Bonding & testing: FNAL, UCSB, Padova, Pisa, Torino, Bari, Firenze, Wien, Zurich, Strasbourg, Karlsruhe, Aachen, HH

Integration into mechanics:

ROD INTEGRATION: FNAL, UCSB

TIB-TID INTEGRATION: Florence, Pisa, Torino

PETALS INTEGRATION: Louvain, Aachen, Brussels, Lyon, Hamburg, Strasbourg, Karlsruhe

Sub-assemblies:

TOB assembly: CERN

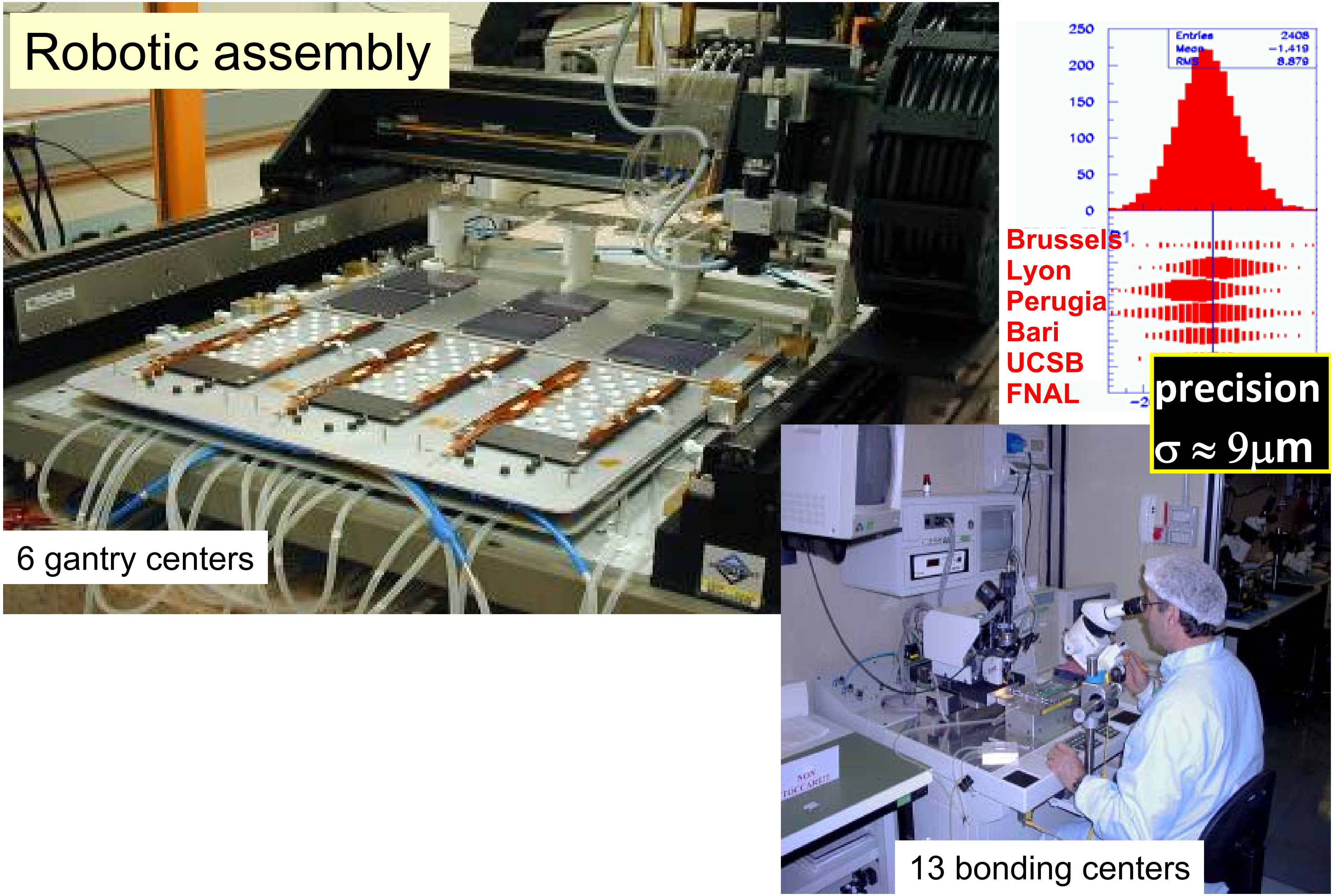
TIB/TID assembly: Pisa

TEC assembly: Aachen

TEC assembly: Lyon@CERN

TK ASSEMBLY CERN TIF → Move to Pit and Insert

Module Production and Test



Robotic assembly

6 gantry centers

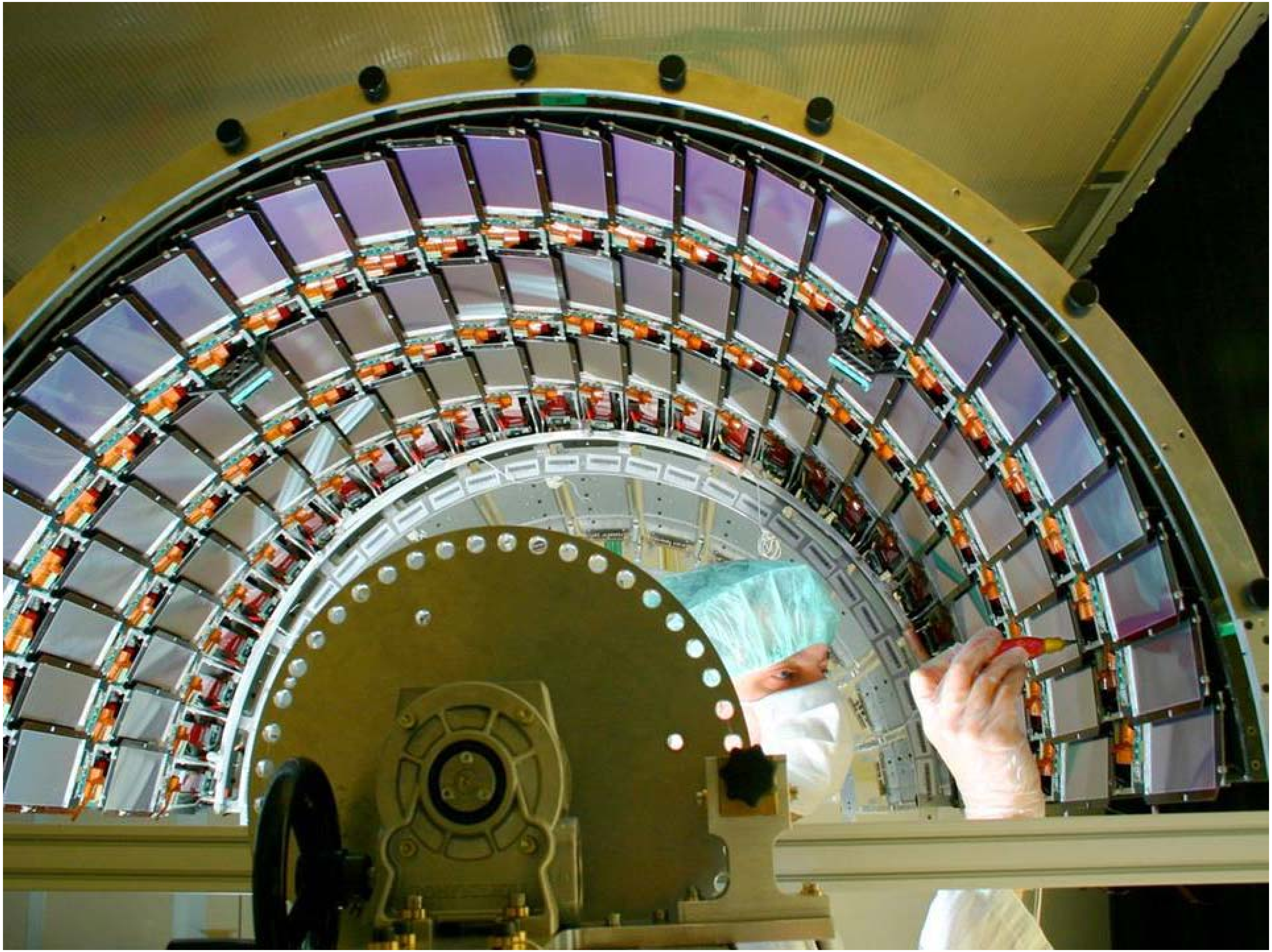
13 bonding centers

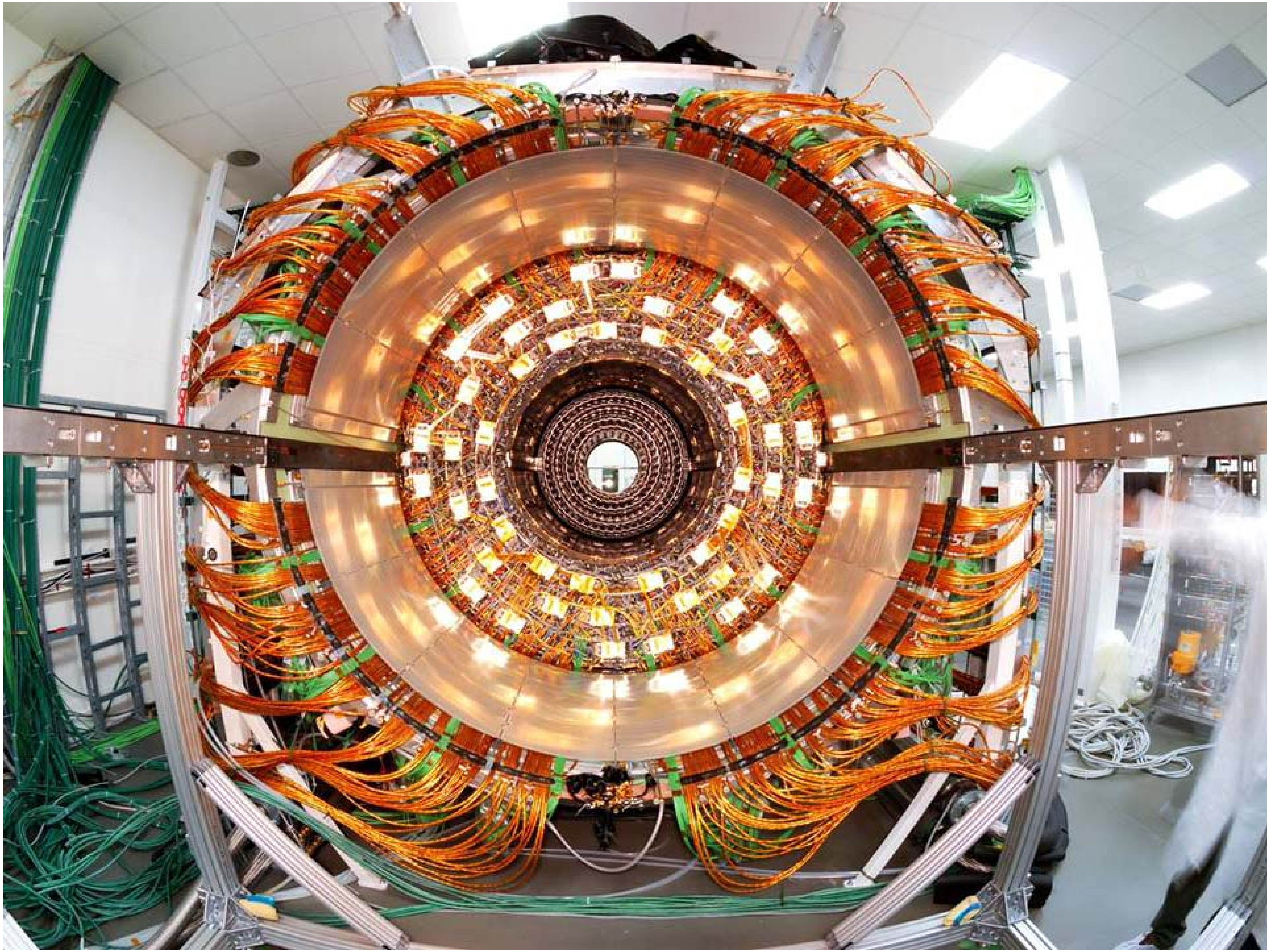
precision

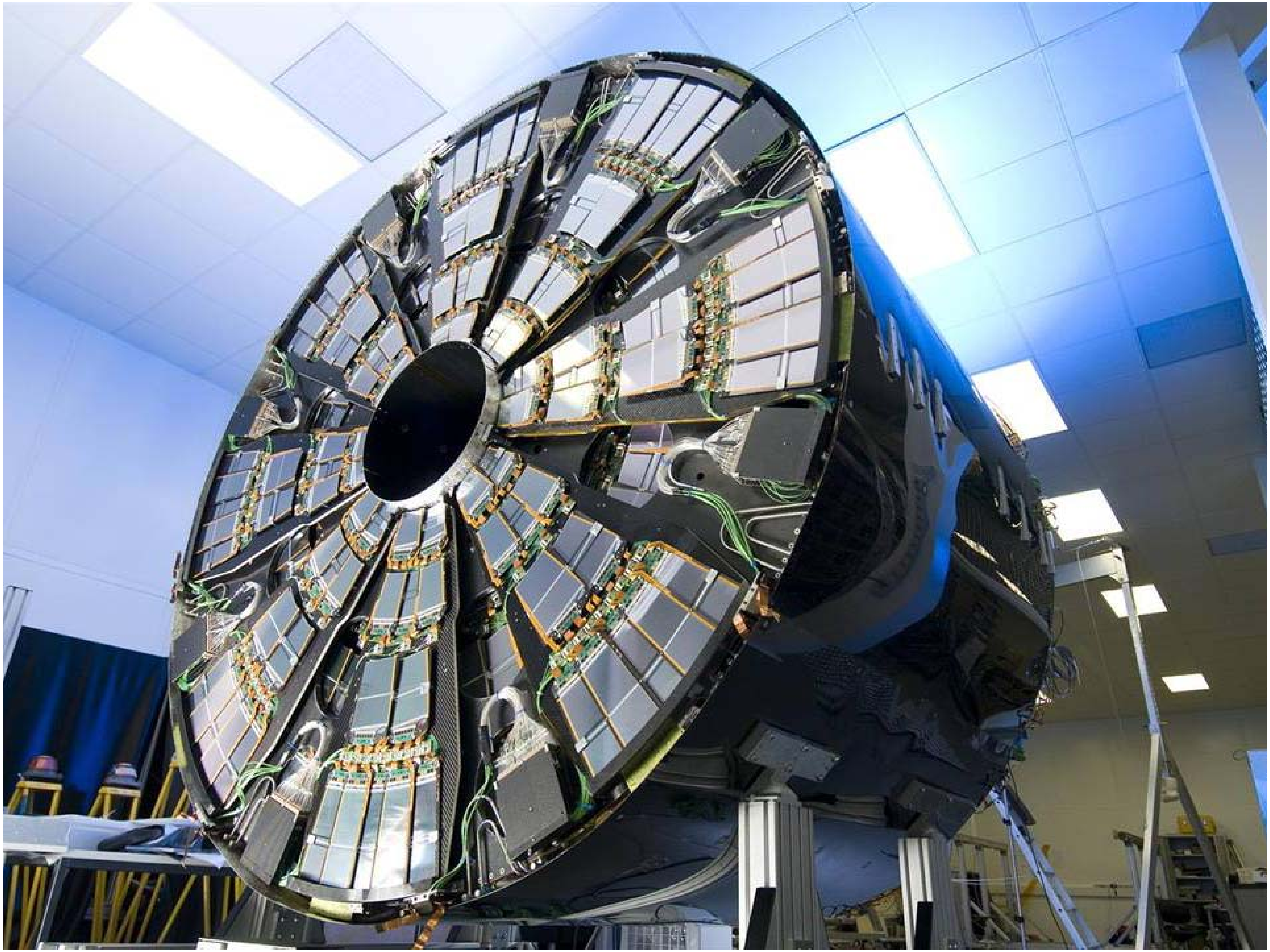
$\sigma \approx 9\mu m$

Intermediate Structures: Petals

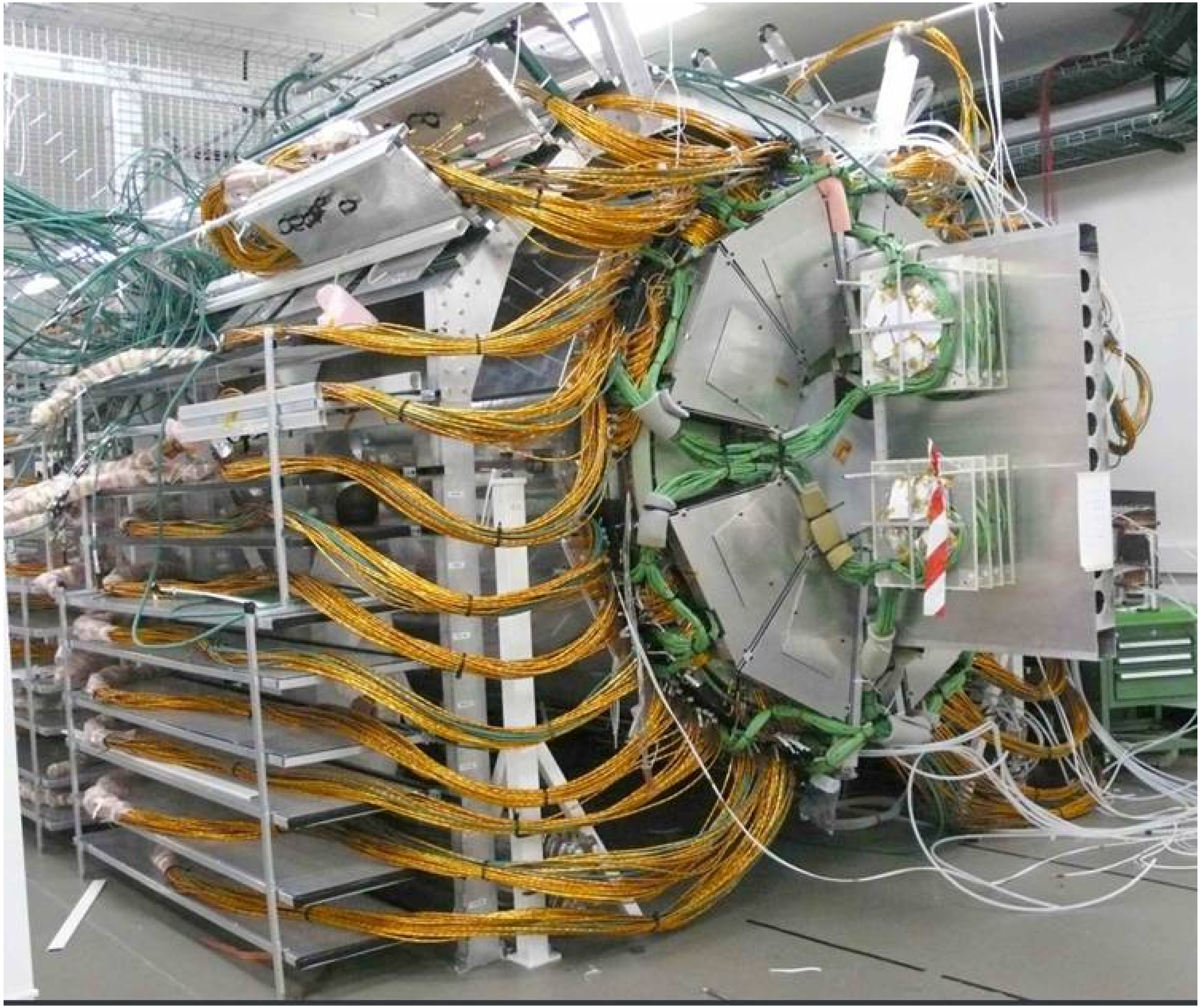
400 Different Pieces Makes one Petal, a Fairly Complicated Object: We needed 288 in total! We assembled 110 in Karlsruhe







Optical Fibres Dressed onto the Tracker



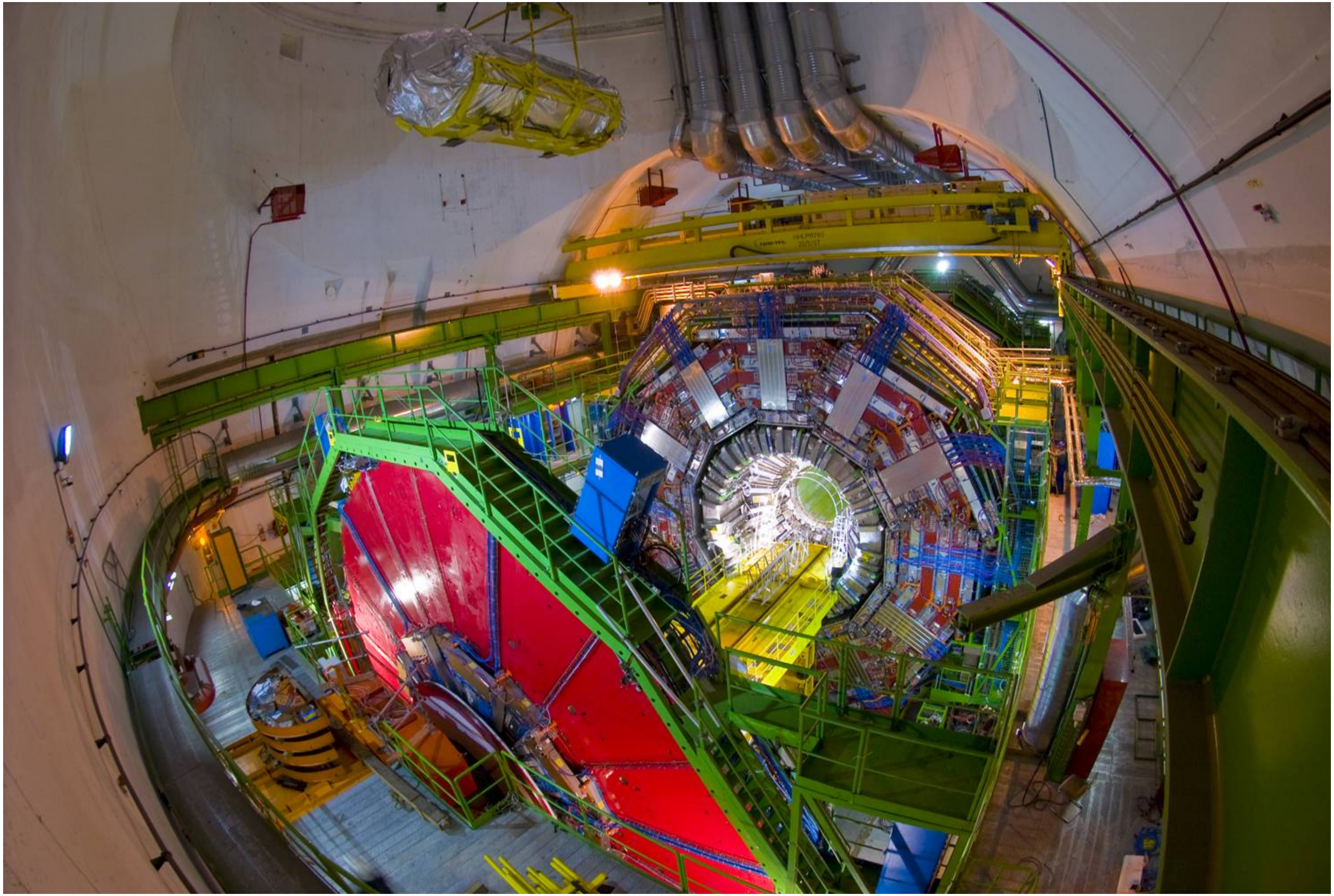
Tracker on the Way Down

- 6.5 tons
- 100 MCHF
- 2000 man years
- 100 m deep shaft below
- Not insured ;-)

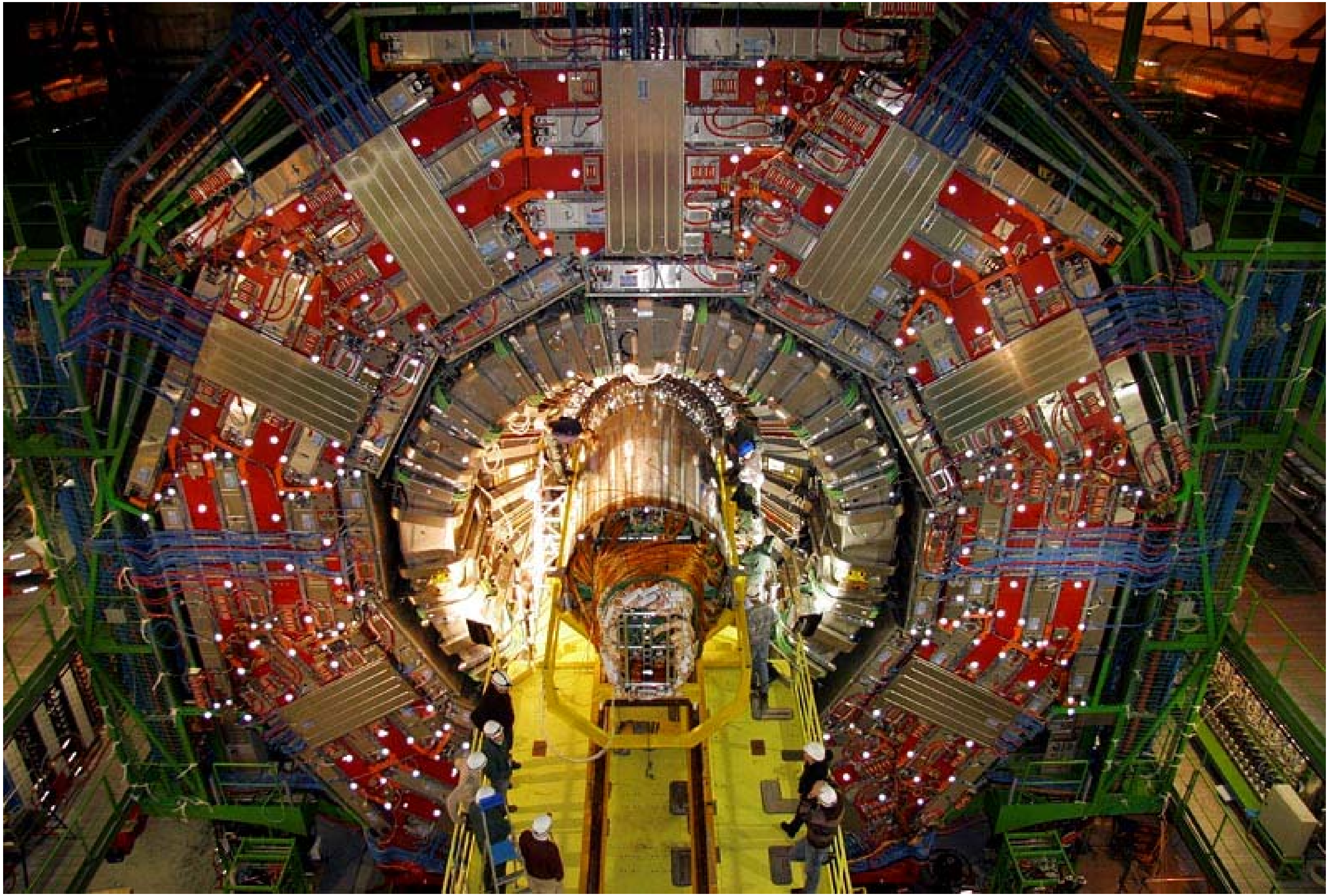
On the hook!

- Several frightened physicists, including me!

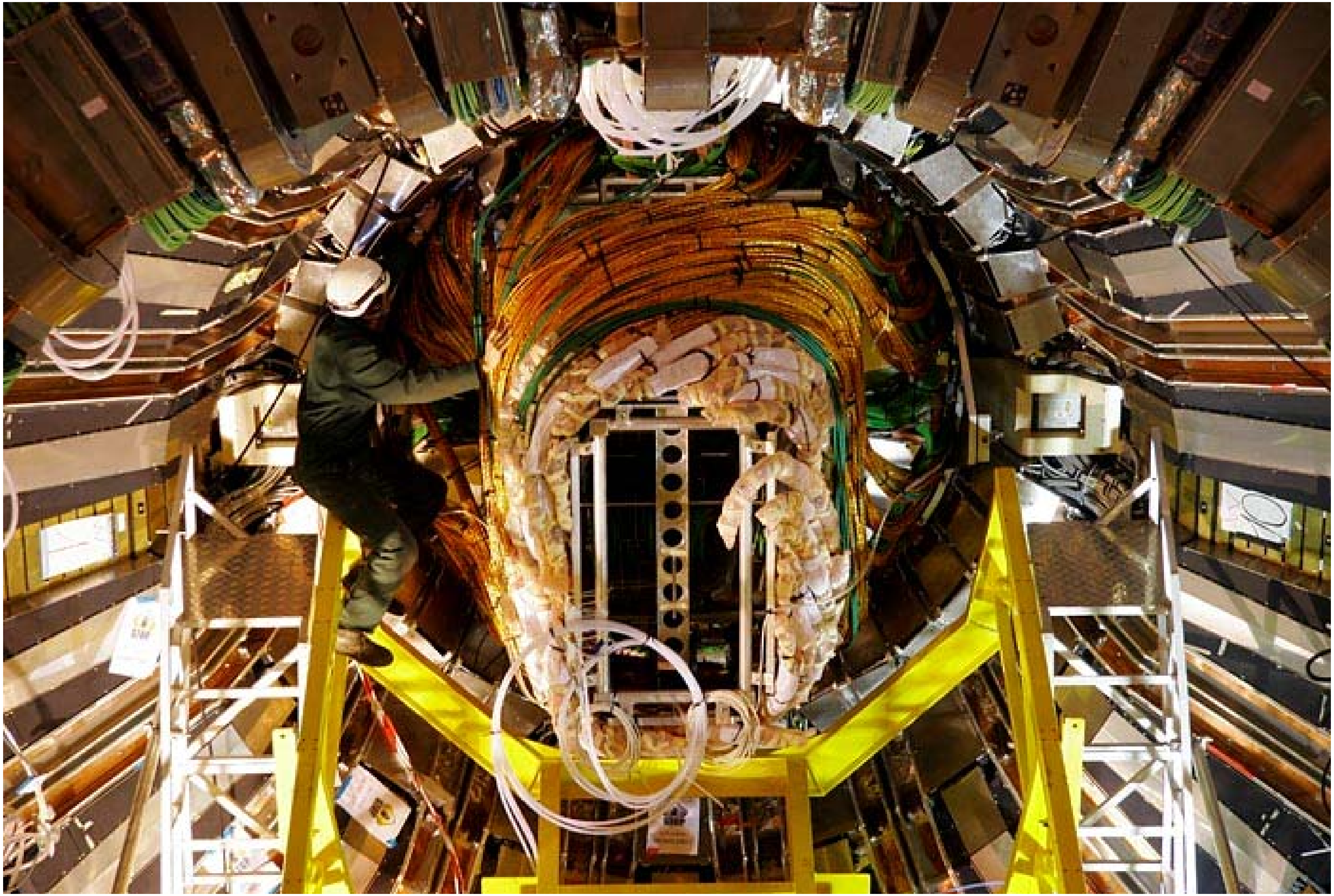
FLY IN



Insertion of the CMS Tracker into the Heart of CMS



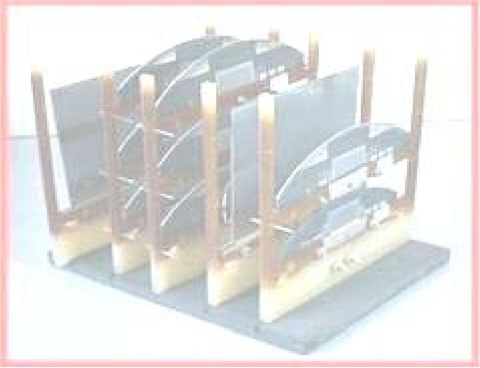
DONE, TRACKER IS IN(Sunday 15.12.07 01.30)



2009: FPIX + removal + repair

Photo: Michael Hoch

KIT irradiation centre



One of the main difficulties is the degradation of the sensor properties under particle irradiation

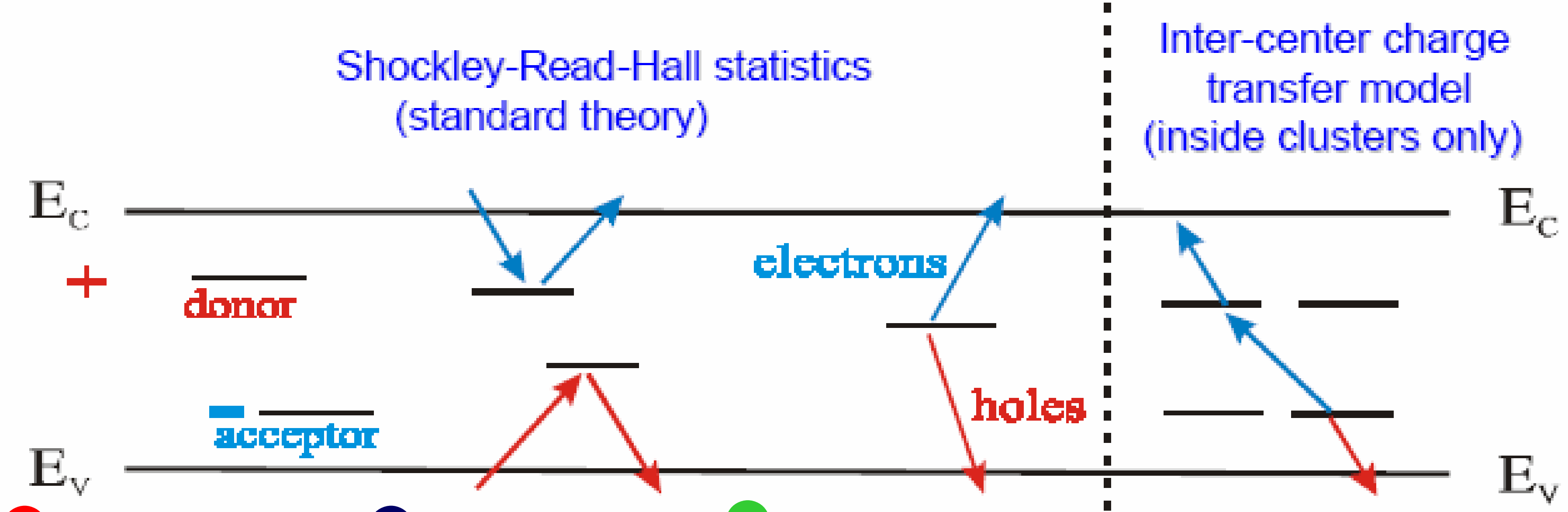
This is the current main topic of research for the SHLC upgrade

RADIATION DAMAGE

Very short (would be a lecture by itself)

Radiation damage
new energy levels in the band gap

1. ● **Change of material type – resistivity – operation voltage**
2. ● **Trapping – loss of charge**
3. ● **leakage current**



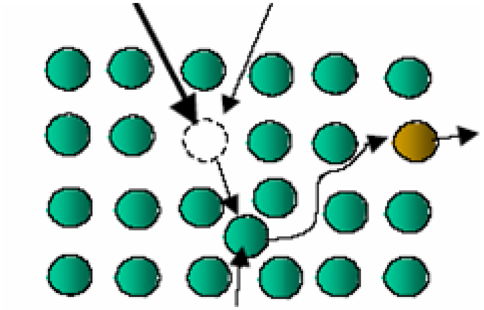
charged defects
⇒ N_{eff} , V_{dep}
e.g. donors in upper and acceptors in lower half of band gap

Trapping (e and h)
⇒ CCE
shallow defects do not contribute at room temperature due to fast detrapping

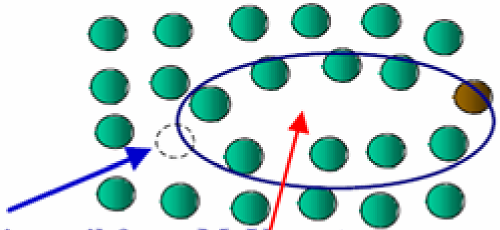
generation
⇒ leakage current
Levels close to midgap most effective

enhanced generation
⇒ leakage current
⇒ space charge

Radiation damage in silicon detectors
Bulk Damage (microscopic)



mobile Interstitial I
creation of point defects



Si recoil from MeV neutron

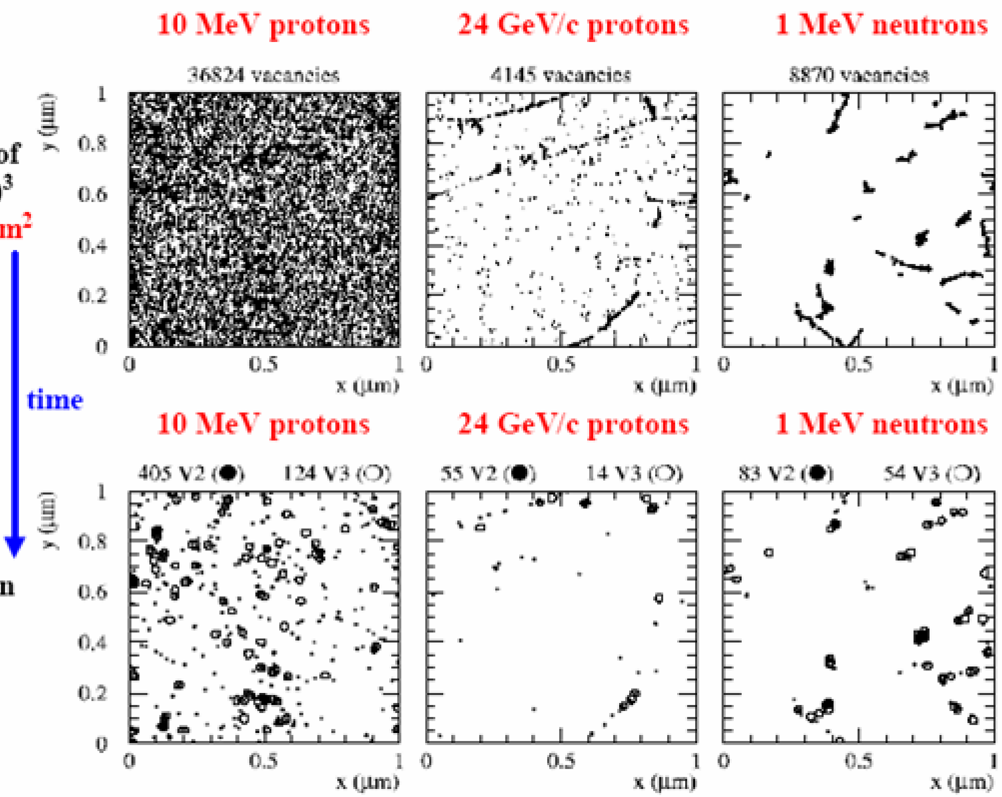
creation of disordered regions, „Cluster“

V, V_2 and V_3 Formation - Particle Dependence

Initial distribution of vacancies in $(1\mu m)^3$ after 10^{14} particles/cm^2

I,V random walk
+
recombination or defect formation

Final constellation of V_2 and V_3



Michael Moll – CERN Detector Seminar, 14 September 2001 - 39

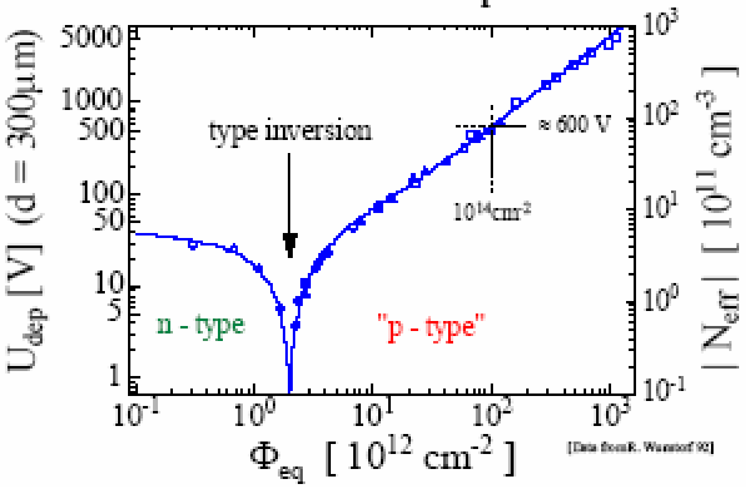
[Mika Huhtinen ROSE TN/2001-02]

Today, we have a reasonable understanding, of microscopic defects corresponding to macroscopic electrical degradation

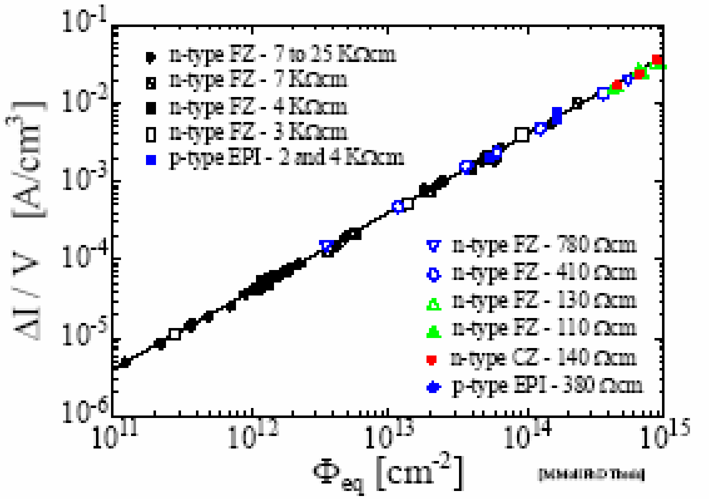
Bulk damage (macroscopic)

Irradiation

1. Change of V_{dep} (N_{eff})



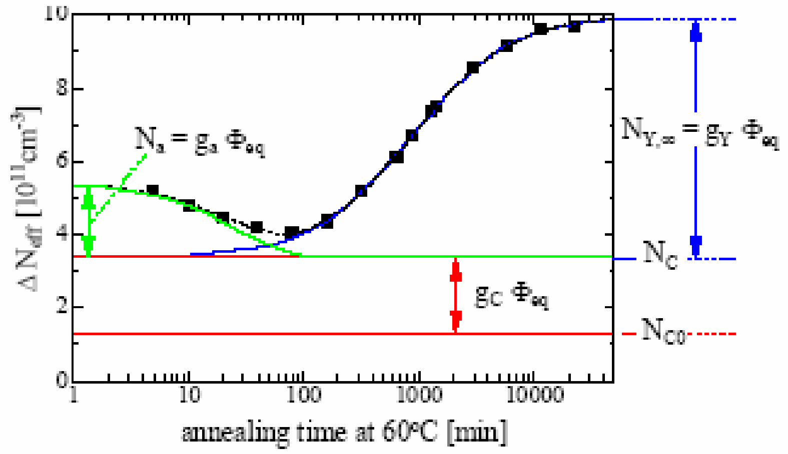
2. Increase of leakage current

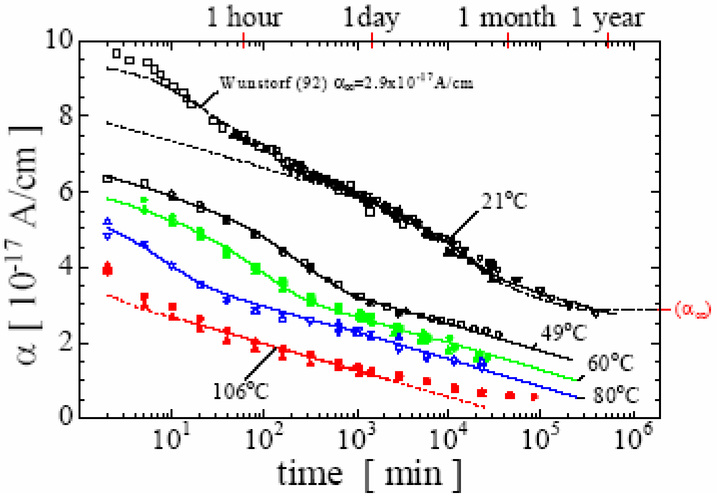


creation of **acceptor** levels = change of resistivity = V_{FD}

creation of mid gap levels = leakage current

Annealing
(e.g. at 60°C)





Annealing ~ diffusion ~ recombination of damages or combination of damages

Annealing strongly dependent on T, therefore LHC detectors running sub-Zero

Radiation effect in electronics (surface damage)

- Main degradations:
  - – *threshold voltage shift of transistor Vthr*
  - – *increased noise*
  - – *increased leakage current*

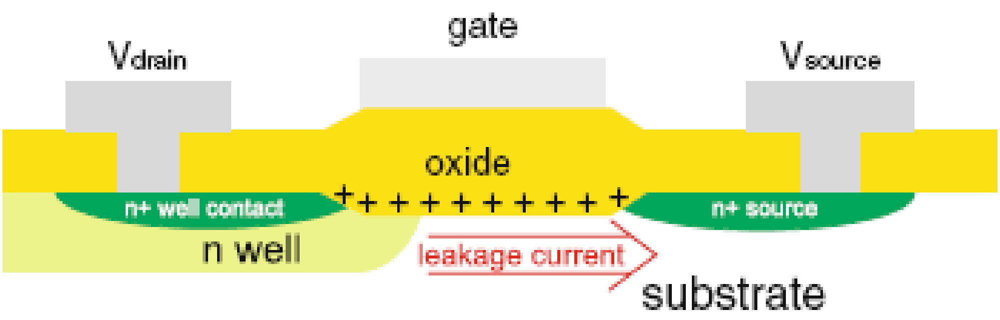
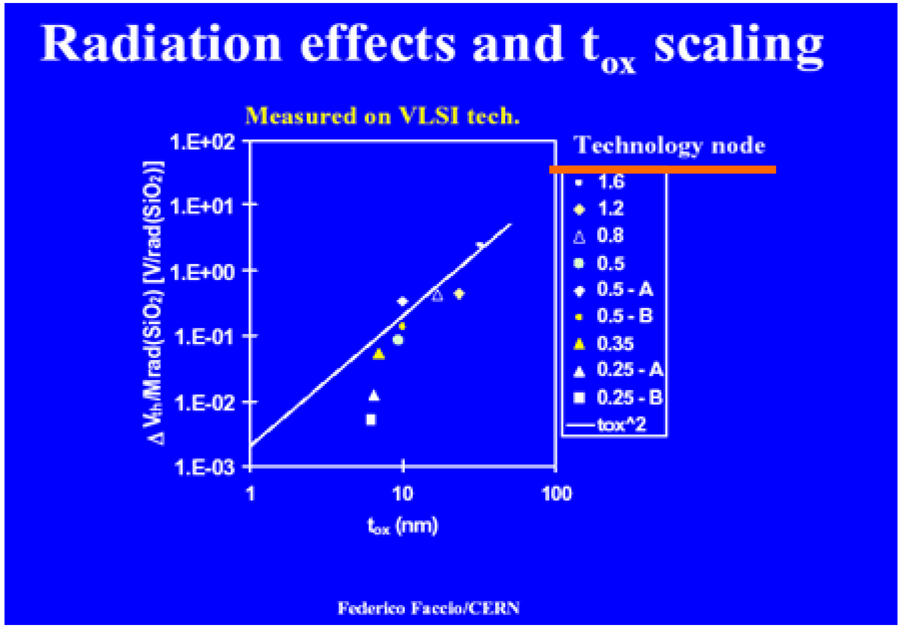


Fig. 1.62 Scheme of an NMOS transistor with deteriorating oxide charge from radiation. The oxide charge screens the gate voltage and therefore a higher threshold voltage V_{thr} is needed to operate the transistor. The resulting attracted charge carriers in the substrate region increase leakage current. The accumulating negative traps in the substrate finally affect mobility. Resulting energy levels in the mid-band region also reduce lifetime and therefore increase leakage current

Readout electronic (Chip)

Just in time for the LHC

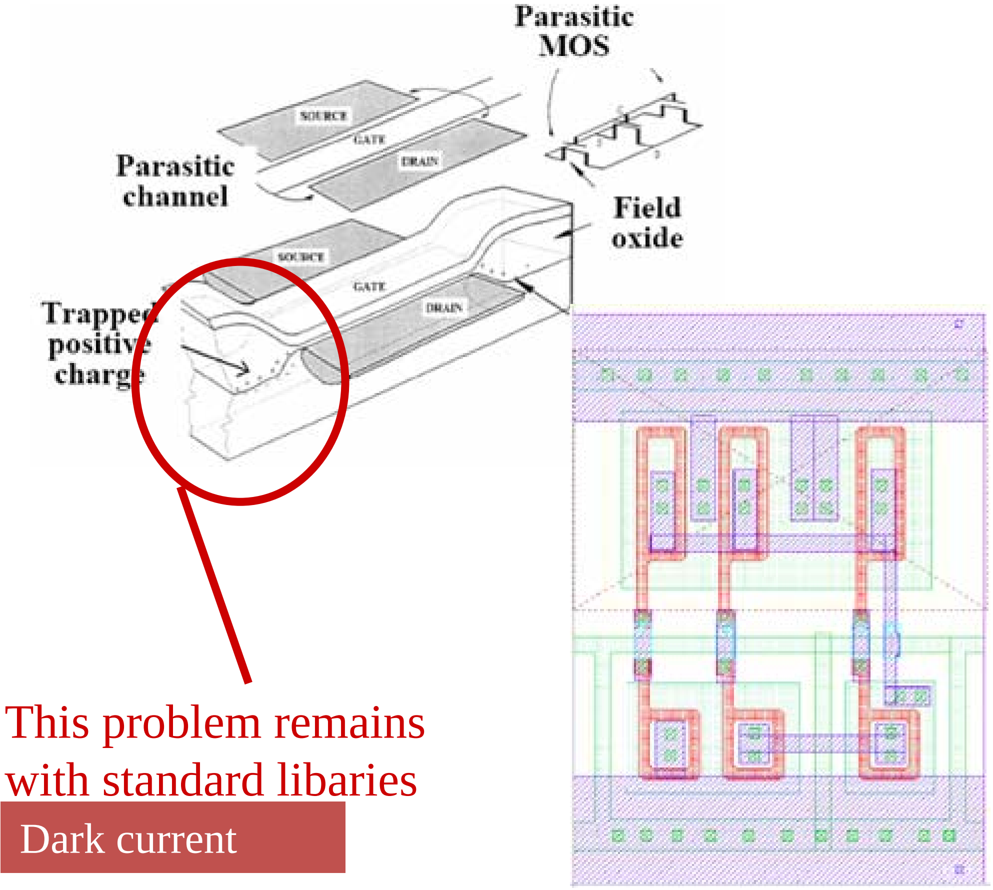


Radiation effects and t_{ox} scaling

Measured on VLSI tech.

Federico Faccio/CERN

The smaller the feature size, the more radiation hard



This problem remains with standard libaries

Dark current

Special libraries: (enclosed geometry)

Source: Frederico Faccio

Charged Coupled Devices (CCD)

Hybrid Active Pixel (HAPS)

Monolithic Active Pixels (MAPS)

Silicon Drift Detectors

Silicon On Oxide (SOI)

3D detectors

Silicon Photo Multiplier (SIPM)

OTHER SILICON DETECTORS

HAPS
Hybrid Active Pixels

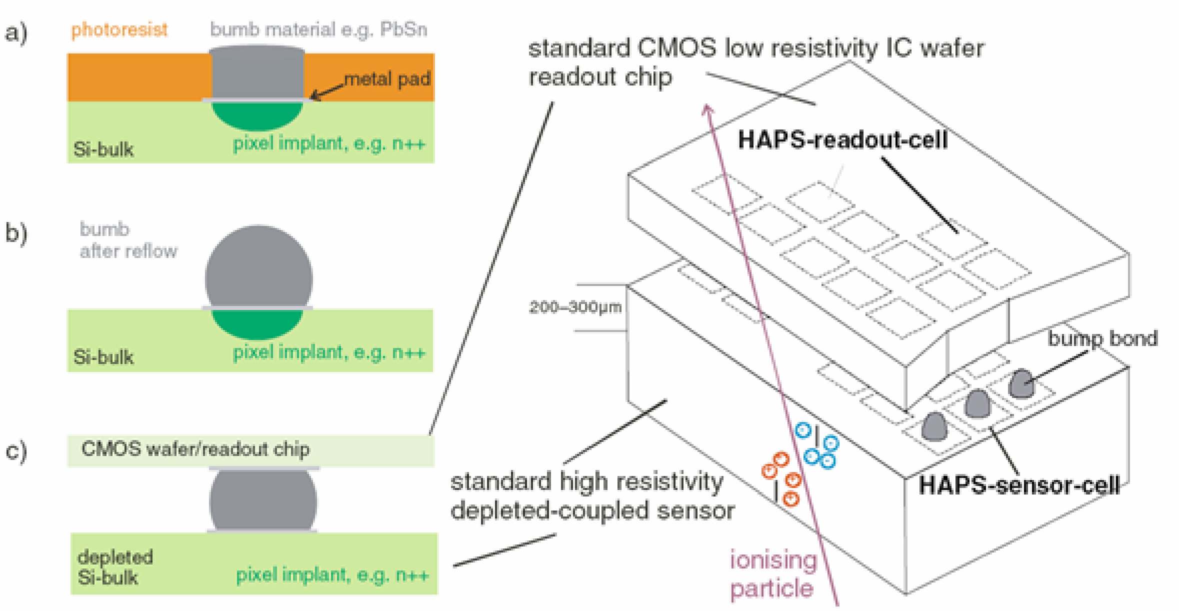


Fig. 1.63 Scheme of a *H*ybrid *A*ctive *P*ixel *S*ensor (HAPS). A HAPS is a sandwich of a silicon sensor and a standard CMOS readout chip. The sensor is of the high resistivity-depleted DC-coupled type processed as described in Sect. 1.8.2. The readout chip is realized in standard CMOS technology on a low-resistivity wafer, the same size as the sensor, and its readout cells are distributed in the same "pixellated" way as the sensor pixels. The merging is realized via so-called "bump bonding" or "flip-chip-bonding". After preparing the pads with a dedicated under-bump metallization a further lithography step opens holes on each pad to place the bump metal (**a**), e.g. Cu or In. After removing/etching the photoresist the metal undergoes another temperature step, the so-called reflow to form balls of metal (**b**). The chip is then "flipped", aligned and pressed onto the sensor, warmed up for reflow, connecting sensor channels to readout cells (**c**)

Used in DELPHI, ALICE, ATLAS; CMS

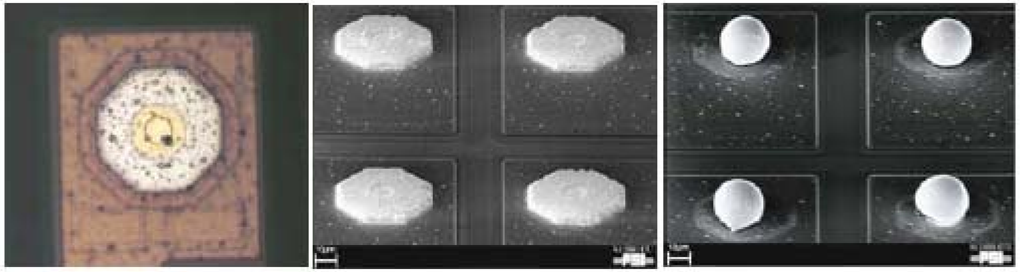


Fig. 1.64 Bump bonding at PSI for the CMS pixel detector. The *left* shows a bare contact on the pixel silicon sensor. In the *middle* part, an electron microscope picture of the structured indium bumps before the reflow process is shown. On the *right*, the bump ball after reflow is shown. The distance between bumps is 100 µm, the deposited indium is 50 µm wide while the reflowed bump is only 20 µm wide [34]

HAPS in CMS

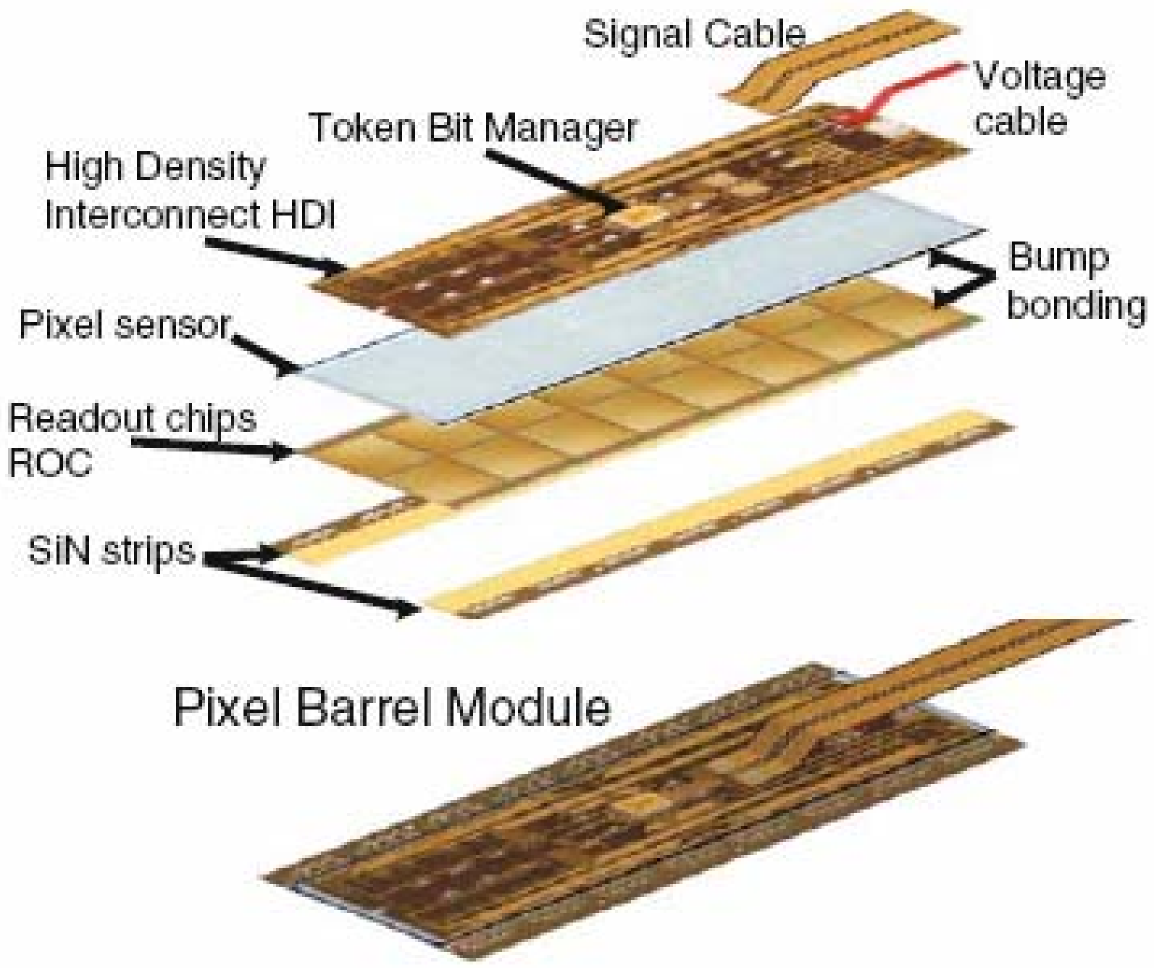
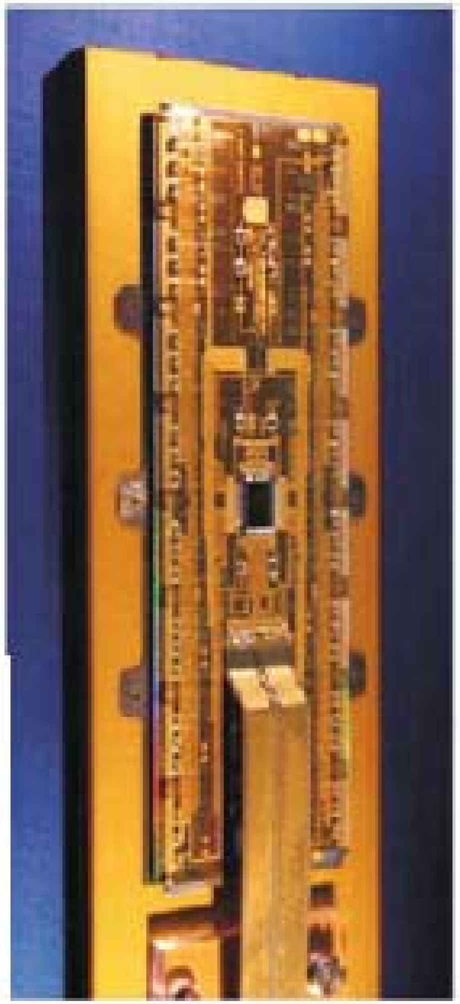
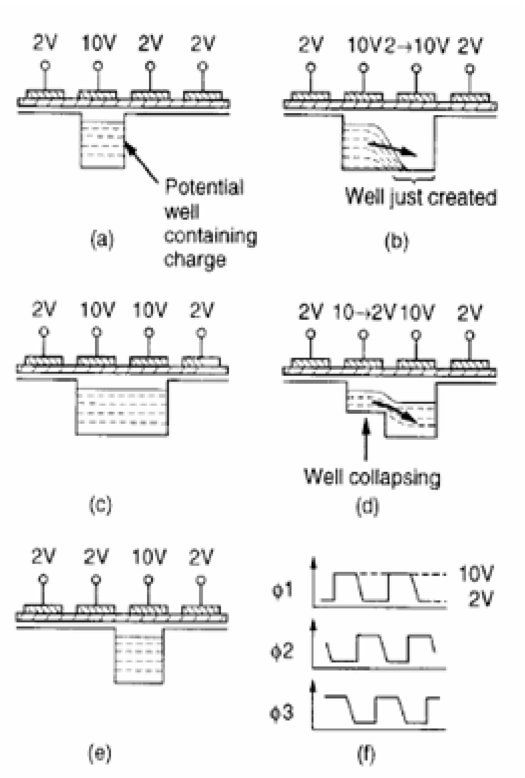


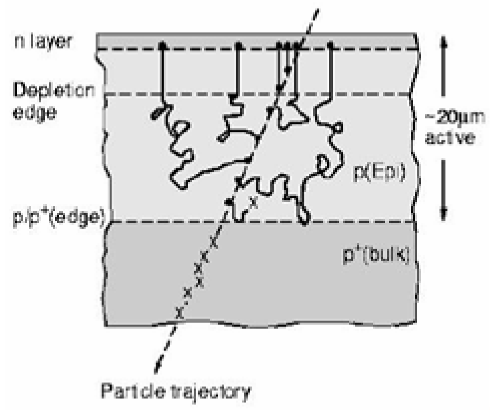
Fig. 5.4 Pixel module – barrel type [44]



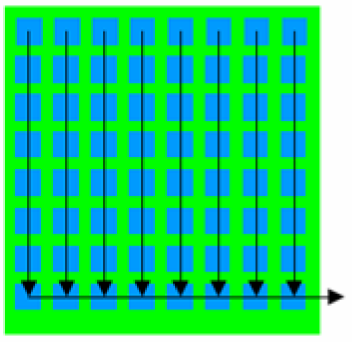
Charge Coupled Device CCD (in older digital cameras)

CCD pixel detectors : Still the active depth is usually quite small (typically 15μm) so the ionization signal is small. The charge is kept isolated in the pixel and then shifted as shown:





Data shift



The SLD silicon pixel vertex detector: the first pixel detector in a collider experiment had 20μm x 20μm pixels and achieved about 4μm resolution.

By changing the potential on the gates in one out of 3 rows at a time, one can achieve a “bucket brigade” effect of shifting the charge to the next “well” without it spreading.

MAPS Monolithic Active Pixels
CMOS (Complementary Metal-Oxide Semiconductor)

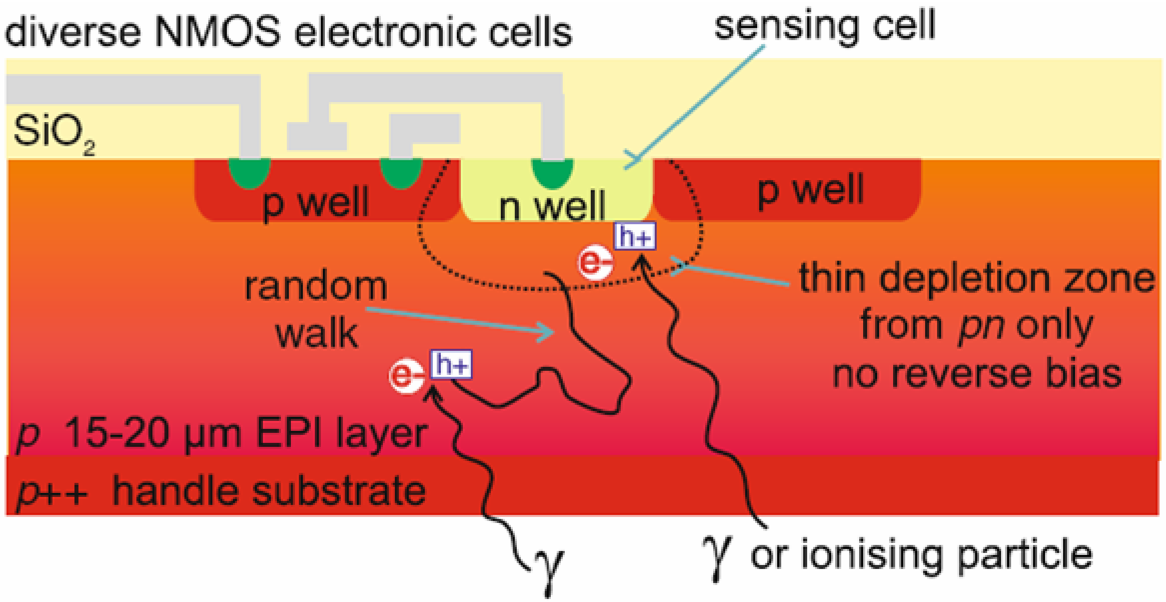


Fig. 1.65 Cross section of a CMOS sensor, one pixel. The scheme nicely depicts an example of NMOS transistors and the N-well to collect electrons from ionization or photo-effect. Electrons created inside the shallow depletion zones are fully collected while electrons from the EPI layer randomly walk towards the N-well and with an excellent lifetime behaviour only some of them will be trapped. Nevertheless, CMOS devices have an excellent signal-to-noise ratio due to their very small capacitances and low currents, therefore the low noise compensates for the low signal

Modern Cameras
Possibly SuperB at SLAC

Silicon On Insulator SOI

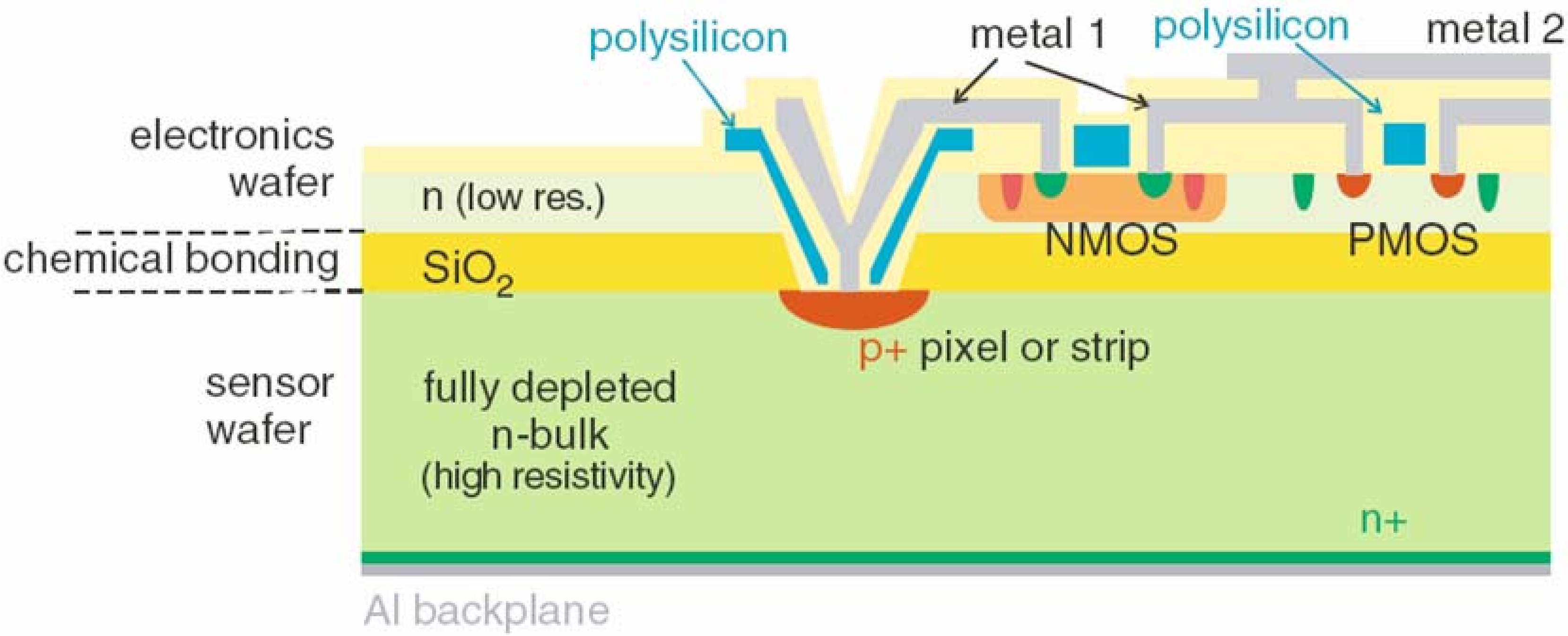


Fig. 1.66 Scheme of a silicon on insulator sensor. The scheme shows the basics of a SOI sensor. Passing charged particles create electron–holes pairs moving to the electrodes in a fully depleted high resistivity *n*-type sensor while the electronics are realized in a low resistivity *n*-type base material, separated by a layer of SiO_2. The connection of both parts is realized by etching while the electronics processing follows standard IC methods. In difference to CMOS devices the sensor wafer can be thick, of high resistivity and depletion is possible. NMOS and PMOS transistors are possible to be processed on the electronics wafer

Silicon Drift Detector

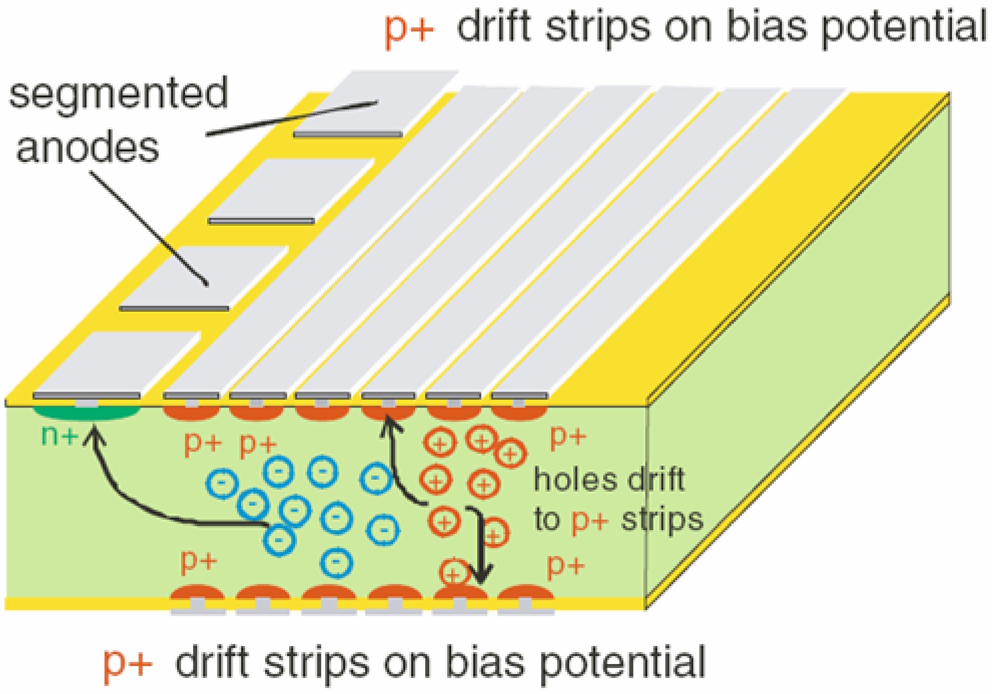
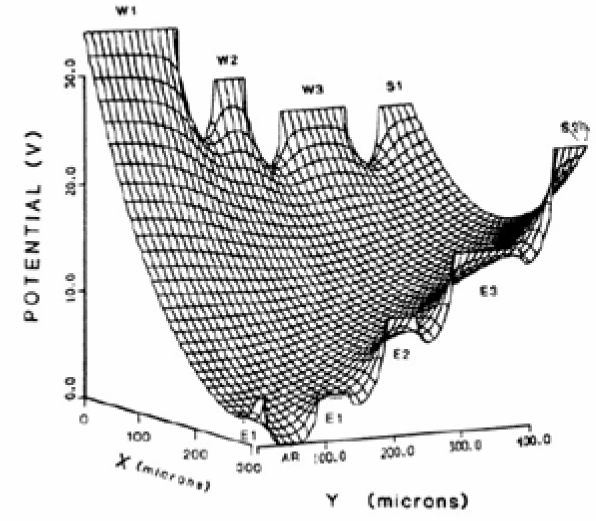


Fig. 1.67 The concept of a silicon drift sensor. Several $p+$ strips on the same potential build a homogeneous field between sensor planes while the edge is structured with $n+$ elements where the free charge carriers drift to; the Y-coordinate is defined by the $n+$ elements while the X-position is defined by the drifting time. Depletion zone builds up horizontally



Used in ALICE

DEPFET Depleted Field Effect

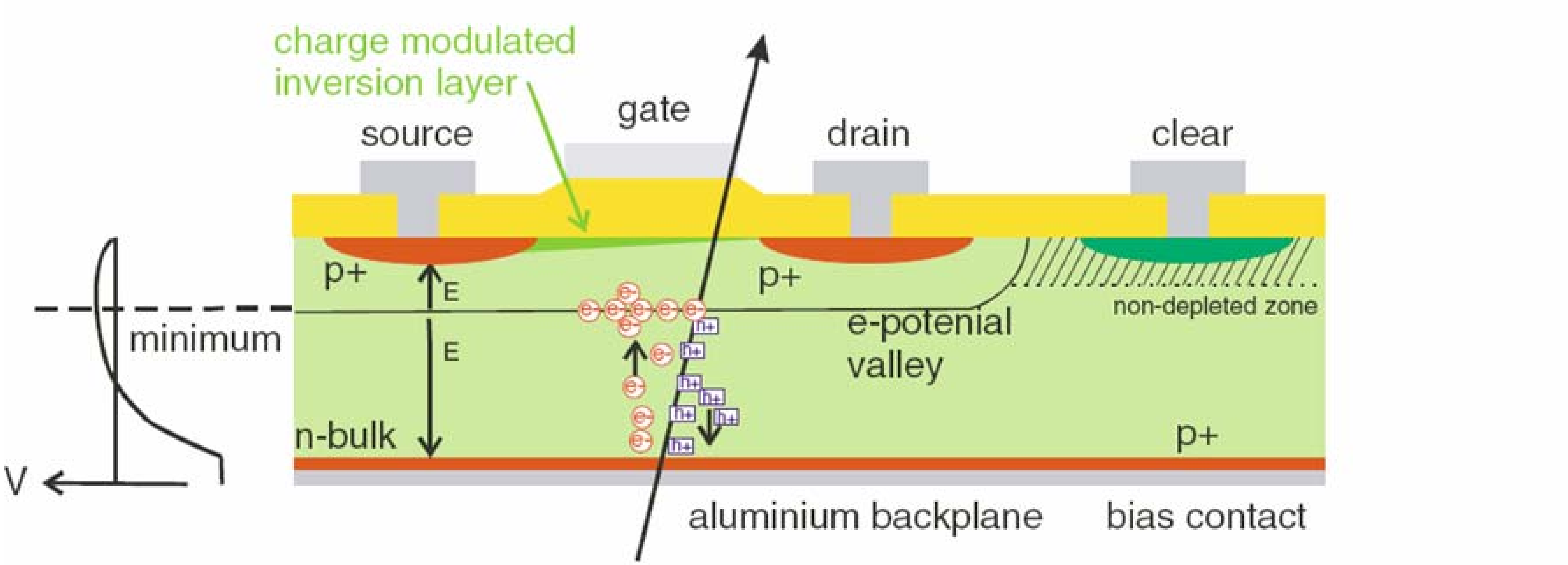
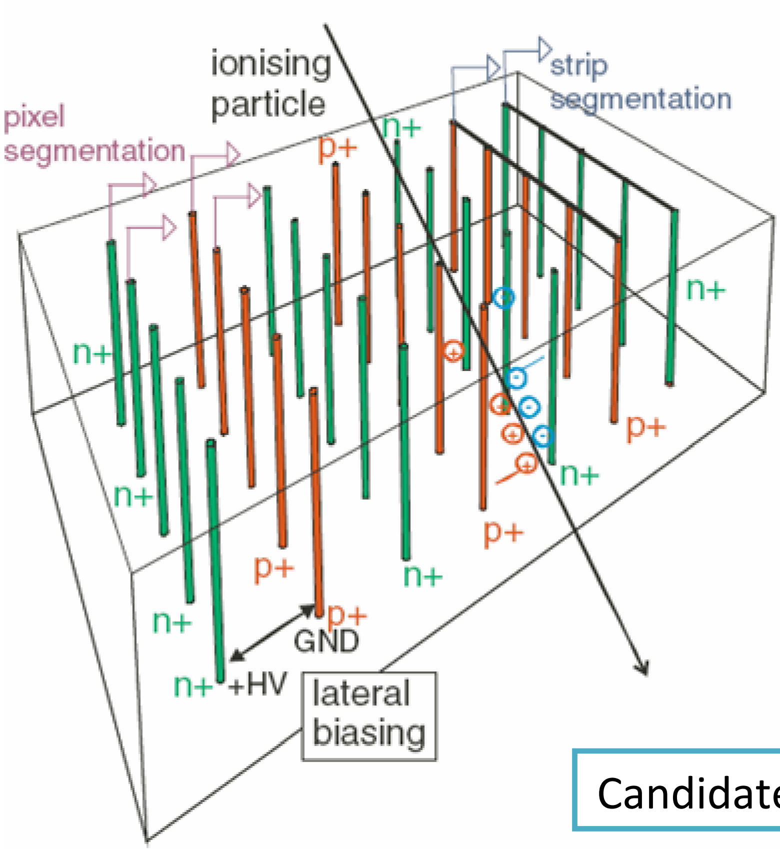
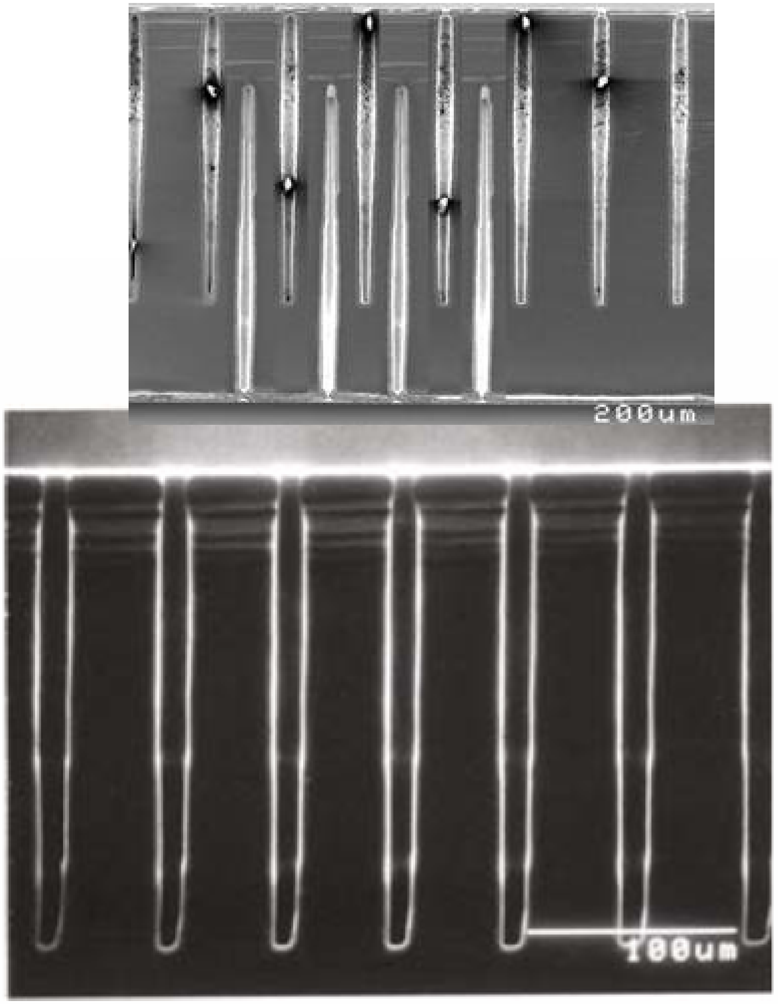


Fig. 1.68 The concept of a DEPFET sensor. The volume is depleted from the side n+ strips down to the back p+ implantation. The potential minimum of the sideways depletion is shifted towards the FET side by optimizing bias configuration. An ionizing traversing particle creates electron–hole pairs in the depleted volume. Holes are lost in the back of the device, while electrons travel to and accumulate at the potential minimum below the external GATE at the so-called internal GATE, thus increasing charge density and thus modulating *source–drain* current of the FET. The electrons stay there until actively *cleared* [111]

Candidate for ILC and SuberBelle

3D detectors





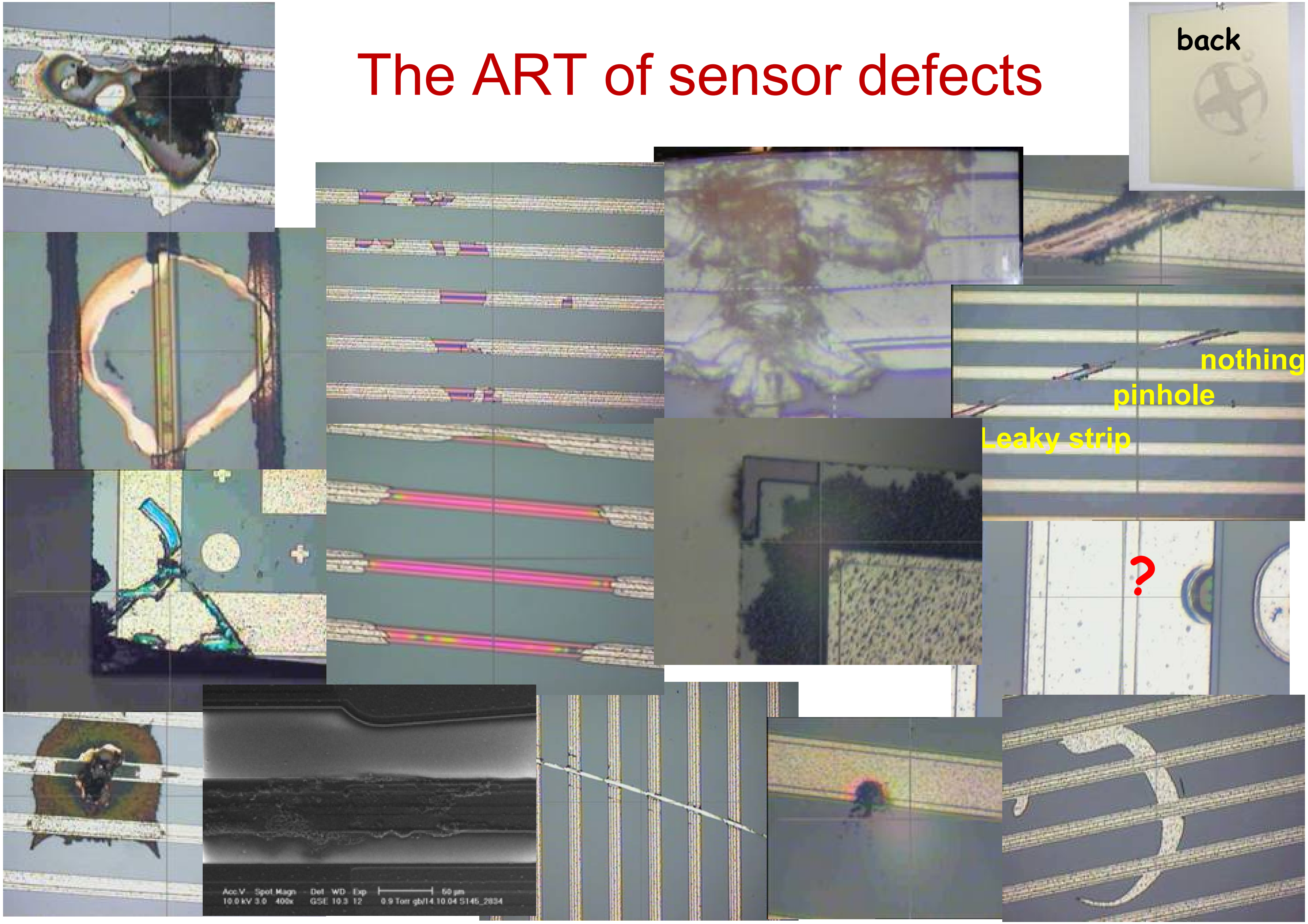
Candidate for inner layers of SLHC

Fig. 1.69 Deviating from the standard planar sensor process deep holes are etched into the silicon to achieve holes, finally serving as electrode junctions to span the depletion zone in a horizontal way instead of the standard vertical one. The electrons and holes travel a much shorter way and are therefore less sensitive to trapping. The pillars can be combined to a strip or pixel pattern. The picture on the right shows a cut through a 3D sensor. Courtesy of CNM-IMB (CSIC), Barcelona [37]

THE END

Thank you very much for your attention

The ART of sensor defects



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- Frank Hartmann http://www-ekp.physik.uni-karlsruhe.de/~hartmann/CMS_Status_Seminar_Bonn1207.ppt